Low- and Ultra Low-Power Arithmetic Units: Design and Comparison

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Abstract

Design guidelines for low- and ultra low-power arithmetic units are presented. We analyze structures for addition in the energy-delay space to determine the most suitable for these regions of operations. This paper demonstrates that the use of more complex high-performance structures combined with scaling of the supply-voltage outperforms traditional low-power oriented designs in the low- and ultra low-power domain.

1. Introduction

Integrated circuit designs for wireless computations and sensor networks are required to operate under ultra low energy requirement. In this design space it is not difficult to find designs which meet the required performance; however the challenge exists in finding the design that uses the least energy for a given performance.

Low power designs have often been compared based on area or total gate count. However, gate count does not account for the impact of transistor sizing and supply voltage scaling on energy and delay. We chose to use adders as a test case to determine if there exists a direct relationship between gate count and the best structures for low power operation.

Recently, two adders have been proposed for low-power and high-speed operation [5,6]. These approaches focus on either improving the energy-delay characteristics of traditional low-power adders through the use of more complex circuits, or simplifying high-performance adders to reduce energy. We analyze these adders in comparison with traditional adders to determine which of these structures are the best for low- and ultra low-power operation.

The paper is organized as follows: in Section 2 we discuss prior work and our approach for design and comparison of arithmetic units; in Section 3 energy efficient adder designs and design considerations are introduced; Section 4 describes the simulation setup; Section 5 presents the comparison of these adders in the low- and ultra low-power domain; and Section 6 concludes the paper.

2. Analysis

Different arithmetic algorithms have been proposed in order to improve computational efficiency in terms of speed, area, and regularity of structures. In low-power applications, evaluating the energy efficiency of the algorithm is crucial. Research for low-power adders lacks the framework for analyzing and quantifying the energy ramifications of different algorithm choices and their implementations.

2.1. Prior Work

Delay estimation of designs was initially based on the number of logic levels. The notion of fan-in and fan-out considerations for the delay was formulated in [7] and later expanded into a comprehensive method known as "Logical Effort" [16]. In [7], different adder implementations are compared in terms of their delay and complexity. Complexity of the adder structure is expressed by the number of equivalent 2-input gates. It was shown in [7] that a structure optimized around the critical path, Variable Block Adder, could reach speed of Carry-Lookahead Adder (CLA) yet with a low complexity comparable to the Ripple-Carry Adder. The gate count and complexity of adder implementations considered in this paper are shown in Table 1.

Table 1. Gate Count and Complexity of Adders

Adder Type (32-bit)	Gate Count	Complexity
RCA	161	208
CSK [13]	197	245
VBA [7]	209	254
CSA [12,15]	248	423
CLSK [5]	272	338
KS [14]	404	461

Neither gate count nor complexity can be used as a figure of merit for energy efficiency because they do not account for the impact of switching activity, gate sizing, parasitics and wiring on energy. Approaches for determining the best adder through the use of more complex figures of merit have been suggested in [9,10].

To evaluate the design, the following figure of merit for "efficiency" of was used in [9]:

$$\text{Efficiency} = \frac{10{,}000}{D \times T} \qquad \text{(Eq. 1)}$$

where D was the worst case delay and T corresponded to the average number of gate transitions per addition. Based on this metric, it was concluded that a carry-lookahead topology was the best. Later analysis of low-power adders examined the use of transistor sizing [10]. Measurements for the worst case delay were extracted from simulation results. Power measurements were obtained from simulations where all the adders had the same clock frequency which was chosen to accommodate the slowest adder, ripple-carry. Since frequency is kept constant for all the adders, the metric employed for comparison is a scaled form of energy-delay product (EDP). These comparisons are made at only a single operating point, and thus do not capture the varying energy-delay characteristics of each adder.

2.2. Energy-Delay Analysis

It is necessary to perform analysis of arithmetic units for the various design points in the energy-delay space [1,2,3] in order to provide a comprehensive comparison over possible design ranges. For low- and ultra low-power operation energy is the primary objective. Using linear delay and energy models for gates, it can be shown that the minimal energy through gate sizing is obtained when minimal gate sizes are used. Further energy reduction is achieved through supply-voltage scaling, which can be used to create the energy-delay characteristics of the adder for the low and ultra-low power regions of operation.

3. Adder Designs for Low-Power

In the following section, adder designs for low-power addition are introduced with considerations for energy efficient implementations.

3.1. Variable Block Adder (VBA)

Carry-Skip-Adder (CSK) was initially proposed to improve the speed of a Ripple-Carry-Adder (RCA) with only a minimal overhead in number of gates [13]. The speed of CSK was improved in the Variable-Block-Adder (VBA) [8], where the blocks sizes were varied to optimally balance the delay between the ripple and carry paths. This improvement in speed requires only a small increase in number of gates (Table 1).

3.2. Carry-Select Adder (CSA)

In CSA [12], each block is evaluated conditionally. When carry-in to a block becomes available, it conditionally selects the carry-out and sum-bits of the block. The critical path of CSA is either the ripple-carry path in the largest block or the worst case carry-select path. The optimal block sizing is chosen such that the delay of the ripple and carry select paths are balanced [15]. The addition can be performed in less stages than VBA, however this comes at the expense of increased branching and more logic gates required for conditional computation.

3.3. Carry-Lookahead-Skip Adder (CLSK)

A modification of VBA was introduced in [5] to further minimize delay by using carry-lookahead logic within the blocks. Group sizing is chosen to balance the delay of each path within the adder. This balancing of delay intends to reduce power consumption by eliminating spurious glitch transitions that occur when the delay of the paths are non-equal. A 32-bit implementation has seven logic levels, each with complex CMOS gates. The results in [5] indicated speed comparable to high-performance 32-bit adders. However, it was not shown how CLSK compared to the adders when energy is taken into account.

3.4. Sparse Carry-Lookahead Adder (SCL)

A sparse carry-tree adder architecture proposed in [6] reduces carry-tree density through the use of 4-bit conditional sum computation [11]. Carry signals are generated for every fourth bit (C_3, C_7, …, C_{23}, and C_{27}). This is opposed to Kogge-Stone adder architecture (KS) [14] which generates carry signal for every bit. In Fig. 1, our implementation of the SCL adder is shown. The wire length on the critical path is reduced in our design compared to [6] and has less branching in the carry-tree.

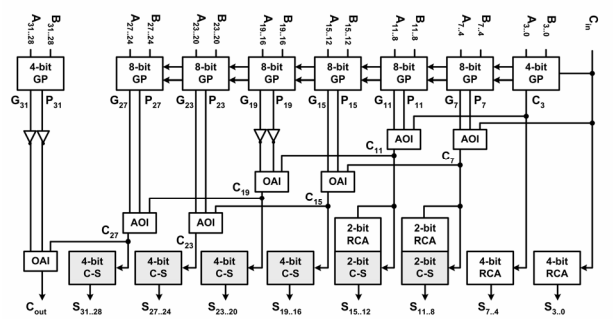

Fig. 1. Sparse Carry-Lookahead adder (SCL)

4. Simulation Conditions

All simulations are performed in a 130nm CMOS technology, with 1.2V nominal supply, at 27ºC, under typical process conditions. The simulation test bench is shown in Fig. 2. Average energy is measured in H-SPICE on a set of 500 random input test vectors. The delay of each adder is obtained from simulation of the critical path vectors.

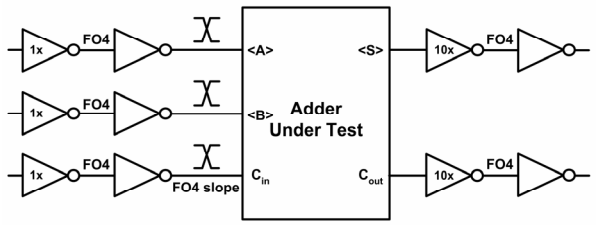

Fig. 2. Simulation test bench

Each output is loaded with a 10µm equivalent gate capacitance. Wire lengths are estimated assuming a 4µm bit pitch and are included in the analysis and simulation. Each adder is sized for minimal energy. Using these gate sizes, the supply-voltage (Vdd) is swept from 1.2V to 0.6V in 50mV decrements to obtain the range of operation for each adder in the energy-delay space.

5. Results

A comparison of the adders at the nominal supply-voltage of 1.2V is shown in Table 2. From this table it appears that VBA is the best design at 1ns, while RCA uses the least amount of energy at 2.1ns. However, it is unclear if these statements will hold if adders are designed to operate at the same delay.

Table 2. Characteristics of the adders at 1.2V

Adder Type (32-bit)	Delay [ns]	Av. Energy [pJ]	EDP [pJ/GHz]	Gate Count
RCA	2.1	1.1	2.31	161
VBA	0.98	1.38	1.35	197
CSA	1	1.78	1.78	209
CLSK	0.94	2.63	2.47	248
SCL	0.62	1.78	1.1	315
KS	0.65	2.04	1.3	404

We use the results of the adders at nominal voltage from Table 2 to define the low- and ultra low-power regions of operation. The low-power region is defined as the range of delay between VBA and RCA at nominal voltage (0.98ns to 2.1ns). The ultra-low power region is defined as the region of operation where delay exceeds the performance of RCA at nominal voltage (>2.1ns), as indicated in Fig. 3, 4.

Simulation results for the energy and delay of the adders described in Section 3 are presented in Fig. 3.

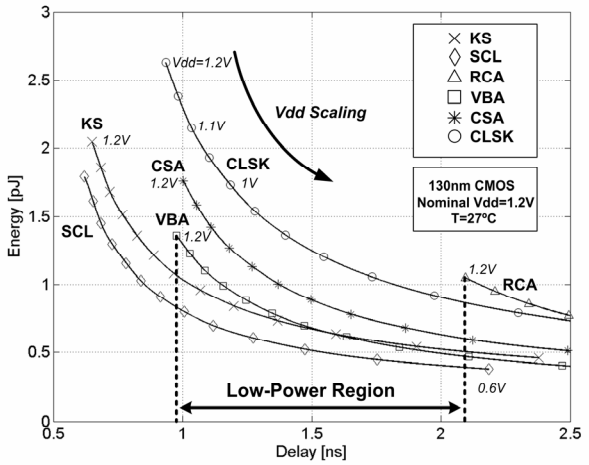

Fig. 3. Low-Power comparison of 32-bit adders with Vdd scaling

In the low-power design region the use of high-performance schemes, such as SCL, combined with reduced supply- voltage always yield lower energy. At the target frequency of 1GHz, the SCL adder can operate at 0.85V and consumes 42% less energy than VBA which must operate at nominal voltage to achieve the same speed. As supply-voltage is reduced, the energy saving of the SCL structure versus VBA is reduced. At the intersection of low-power and ultra-low power region, which occurs at 2.1ns, the energy saving of SCL compared to VBA is 25%.

The results in Fig. 3. also demonstrate that CLSK which was designed as intent to reduce power and yet improve performance, is inefficient in all regions of its operation. It leads to only 5% of delay improvement over VBA at the expense of twice the energy consumption. Among traditional low-power designs, the CSA structure demonstrates similar performance to VBA, however conditional computation led to an energy increase of 30% compared to VBA.

Simulation results for the ultra low-power region of the adders are shown in Fig. 4. At the lowest operating voltage (0.6V), VBA is two times faster than RCA and requires only a 25% increase in energy. At nominal voltage, there is no justification of using simple RCA structure, it has 2.5x higher energy than SCL adder operation at 0.6V, thus provides no energy savings at all.

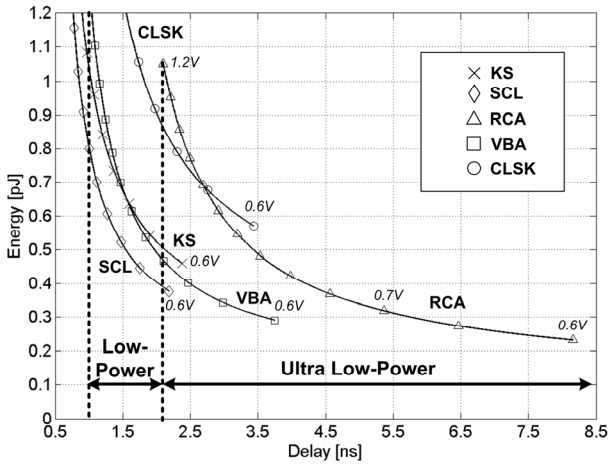

Fig. 4. Ultra low-power comparison of 32-bit adders with Vdd scaling

6. Conclusion

In this paper, we provide an approach for the design and comparison of 32-bit adders for low- and ultra low-power applications. The energy-delay space results demonstrate that when designing for low power a comparison of designs at a single voltage or a comparison based on gate count is insufficient for determining the optimal structures.

We have demonstrated that the use of high-performance structures combined with supply-voltage scaling, results in reduced energy compared to traditional designs for low power and ultra low-power operation. This finding is contrary to common belief.

7. Acknowledgements

This work has been supported by SRC Research Grant No. 931.001, California MICRO 04-068, Fujitsu Ltd. and Intel Corp.

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