COMPARATIVE ANALYSIS OF DOUBLE-EDGE VERSUS SINGLE-EDGE TRIGGERED CLOCKED STORAGE ELEMENTS*

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ABSTRACT

We are presenting a comparison of Double-Edge Triggered clocked Storage Elements (DETSE) with their single-edge triggered counterparts in terms of delay and power consumption. In general, Latch-Mux based DETSE perform better then their single-edge counterparts while double-edge triggered flip-flops exhibit performance degradation. Up to 15% improvement in Energy-Delay Product (EDP) of Latch-Mux designs is achieved when using DETSE. Presented results indicate that the use of DETSE is a good choice when low-power operation is required.

1. INTRODUCTION

A commonly used method to improve performance is to increase the clock frequency. However, use of high clock frequency has a number of disadvantages. Power consumption of the clock system dramatically increases and clock uncertainties take significant part of the cycle. Other problems include degradation of the clock waveform due to the non-ideal clock distribution, power supply noise and cross-talk.

An alternative clocking strategy relies on the use of storage elements capable of capturing data on both clock edges (rising and falling edge). Such storage elements are referred to as Double-Edge Triggered clocked Storage Elements (DETSE). In this case, the same data throughput can be achieved with half of the clock frequency.

However, there are three main drawbacks of DETSE: (1) potential increase in the design complexity (2) degraded performance in terms of speed and/or power consumption, (3) control of the clock duty cycle. Today's PLL's mainly control the active (usually leading) edge jitter, while less attention has been paid to reducing the other (trailing) edge uncertainties. Precise duty cycle control is considered essential for efficient operation of DETSE.

The previous work consisted of individual design contributions. So far, little attention was paid to comparison of double-edge versus single-edge clocking strategies. This paper presents one-to-one comparison between several representative DETSE, and their single-edge counterparts Single-Edge Triggered clocked Storage Elements (SETSE). The comparison intends to give arguments for and against the use of DETSE strategy and to provide some directions for further research.

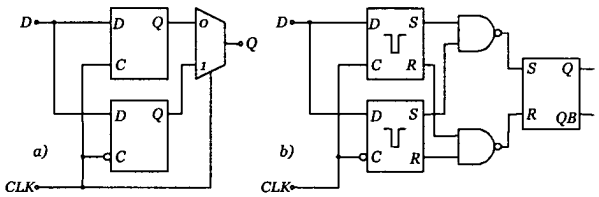

Fig. 1. Basic types of double-edge triggered storage elements a) latch-mux and b) flip-flop

2. STORAGE ELEMENTS USED FOR COMPARISON

Double-edge triggered storage elements can be classified as a Latch-Mux (LM), Fig. 1a, or a flip-flop (Fig. 1b) structure. LM structure consists of two latches, which are transparent on opposite clock phases, and a multiplexer that selects the output of the non-transparent latch, as shown in Fig. 1a. Single-edge counterpart of the LM structure is Master-Slave (MS) latch. Flip-flop structure consists of two pulse generators, each active on different edges of the clock, and a latch that captures the pulses.

The set of DETSE chosen for comparison consists of two best performing storage elements from each of the classes described. Each DETSE is compared to its single-edge version. The set of storage elements follows:

1) *Transmission Gate MS latch* (TGMS, [1], Fig. 2a) and *double-edge latch-mux* (TGLM, [2], Fig. 2b).

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2) *Modified C²MOS MS latch* ([3], Fig. 3a) and *double-edge latch-mux* ([4], Fig. 3b).
3) *Transmission gate flip-flop* (TGFF). Single-edge triggered flip-flop is shown in Fig. 4a. A modification of DETSE from [5] shown in Fig. 4b. We use static flip-flop employing transmission gates, which is different from the original design [5]. This allows us to observe double-edge versus single-edge flip-flop comparison without interference of unnecessary delay degradation of DETSE from [5].
4) *Dynamic True Single Phase Clock Latch* (TSPC [6] in Fig. 5a and double-edge ([7], Fig. 5b).

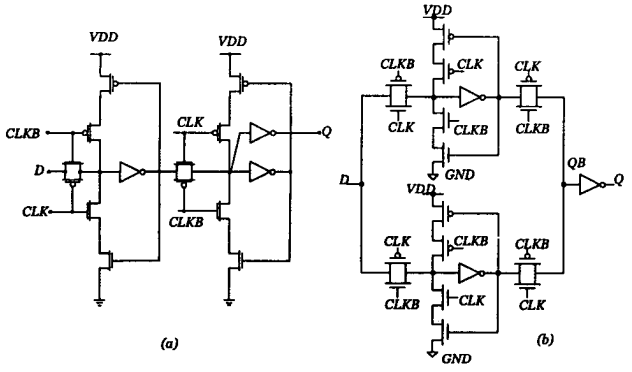

Fig. 2. a) Transmission Gate Master-Slave Latch and b) Transmission Gate Latch-Mux

3. SIMULATIONS AND TESTBENCH

All simulations are produced using 0.18μm Fujitsu technology, power supply voltage of 1.8V and temperature T=25°C. Clock frequency used in simulations is 250MHz for DETSE and 500MHz for SETSE, thus, maintaining the same data throughput. Test-bench used for simulation is shown in Fig. 6. The parameter used as a figure of merit is Energy-Delay Product (EDP). EDP is obtained as a product of delay, clock period and average power consumption with 50% data activity with respect to the maximum throughput. The circuits are sized for minimal EDP. Power used to drive clock and data are included in the total power consumption [8]. In this way, a load imposed by the clocked storage element is included.

The timing metrics used for DETSE [9] will be described briefly: The storage element is characterized with two parameters, determining its overheads in the two ('high' and 'low') half-cycles of the clock:

$$t_{D1} = t_{CLK\text{-}Q,LH} + t_{D\text{-}CLK,HL}$$
$$t_{D2} = t_{CLK\text{-}Q,HL} + t_{D\text{-}CLK,LH}$$

Here, t_{D1} and t_{D2} are two different delays taken from the half-cycle when the clock is at 'high' and 'low' level, respectively. The timing metric (t_{FF}) is the worst-case of the two:

$$t_{FF} = \max(t_{D1}, t_{D2})$$

During the circuit optimization process, t_{FF} reaches its minimum and $t_{D1} \approx t_{D2}$. Times $t_{D\text{-}CLK,LH}$ and $t_{D\text{-}CLK,HL}$ that correspond to minimum of t_{FF} are referred to as optimal setup times, $t_{su,r}$ and $t_{su,f}$ respectively. t_{FF} represents delay of the dual-edge triggered storage element.

Single-edge triggered flip-flops are characterized by their minimum data-to-output time at optimal setup time [8].

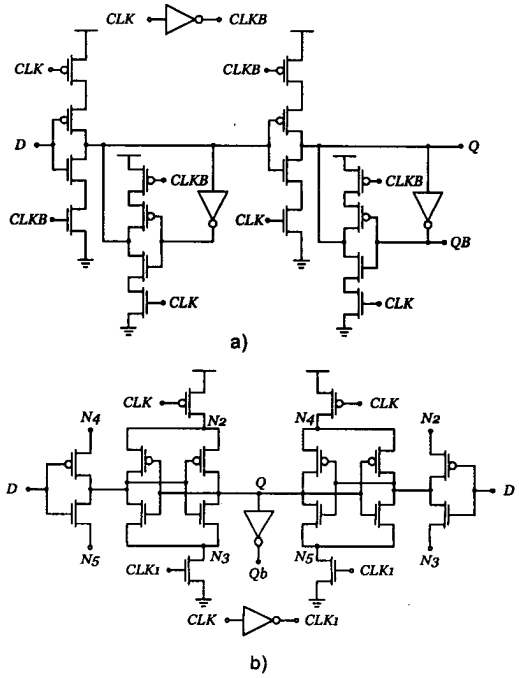

Fig. 3. C²MOS a) single-edge master-slave latch and b) double-edge latch-Mux

4. RESULTS AND DISCUSSION

Simulation results are given in Table 1. Parameter t_{su} is the optimum setup time (in case of DETSE, setup times corresponding to both clock edges are given: $t_{su,r}$ and $t_{su,f}$). Parameter t_D represents the delay of a storage element (for DETSE, delays in both clock half-cycles are given: t_{D1} and t_{D2}). Internal power consumption P_I, includes the power dissipated for the transitions of internal nodes and charging/discharging the output load. Data power, P_D, and clock power, P_{CLK}, represent the dissipation of the data and clock drivers, respectively. Total power consumption,

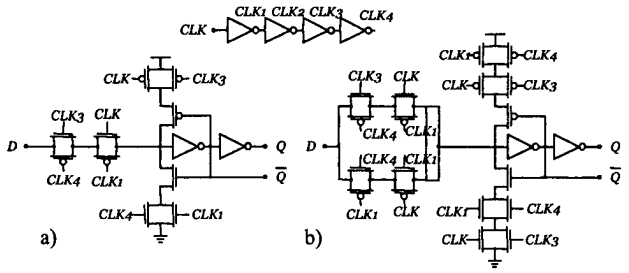

Fig. 4. Transmission Gate Flip-Flop a) single-edge and b) double-edge version

P_{TOT}, is a sum of internal, data and clock power. Overall comparison parameter is the Energy-Delay Product, EDP, computed as a product of total power, delay and clock period.

Fig. 7 and Fig. 8 present delay and EDP comparisons respectively. Simulation results show that single-edge master-slave designs are more suitable for transferring into double-edge structures. This observation is supported by the EDP improvements (3% and 15%) of TGLM and C^2MOS double-edge latches, compared to corresponding single-edge master slaves (TGMS and single-edge C^2MOS). The most significant reason for this is delay advantage of latch-Mux double-edge structure over single-edge Master-Slave latch (critical path from input D to output Q *or* $\overline{Q}$ consists of a latch and a MUX, compared to two latches in SETSE). This advantage can be directly seen in the delay improvement (C^2MOS), or it can be used for the power reduction by appropriate transistor sizing (TGLM vs. TGMS). The performance loss due to a more complicated circuit is minimal here and is overpowered by operating at half the clock frequency which results in decreased power consumption. Optimal setup times of double-edge triggered structures are smaller (better) than those of single-edge master-slave designs.

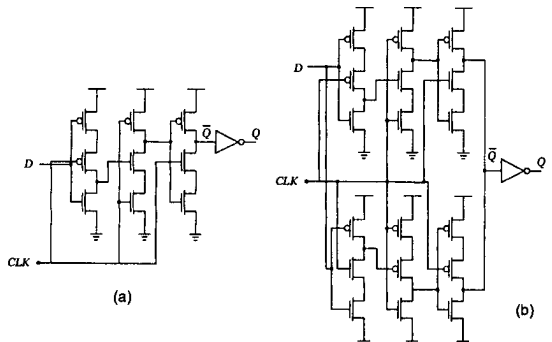

Fig. 5. True Single Phase Clock Latch a) single-edge and b) double-edge version

The performance of flip-flop-based designs (TSPC and TGFF) is inferior to that of corresponding single-edge triggered structures. The main reason for this is the large design complexity increase of DETSE, which results in

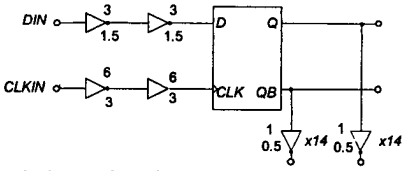

Fig. 6. Simulation tesbench

both delay and power consumption increase. The obvious example is TSPC, where the number of transistors of DETSE is doubled compared to that in SETSE. In addition, critical path on falling clock edge mostly goes along pMOS transistor stacks, which introduces the asymmetry between sub-circuits active on rising and falling clock edge. Overall performance comparison between DETSE and SETSE in this case shows about 43% worse EDP of DETSE as a result of mentioned effects. Table 1. also shows that clock-related power consumption is increased by about 50% despite running at half of the clock frequency. This is due to more than doubled clock load compared to SETSE realization.

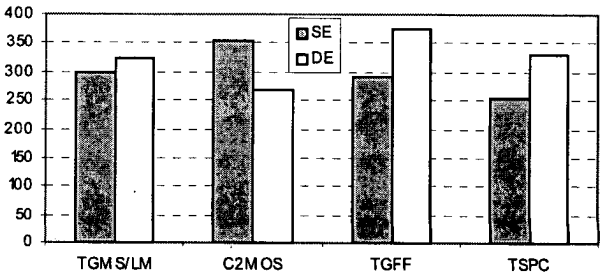

Fig. 7. Delay comparison (time in ps)

Double-edge TGFF complexity overhead is smaller than that of TSPC. As a result, EDP degradation in the case of double-edge TGFF is about 25%, as compared to its single-edge version. Here, reduced clock frequency roughly compensates for bigger circuit, which results in similar power consumption of double- and single-edge TGFF (Table 1). Consequently, only larger delay accounts for EDP degradation. Like TSPC, optimal setup time remains the same.

Fig. 9 shows the power consumptions of the compared circuits when input switching activity changes. Similar to master-slave latches, power consumption of latch-Mux structures is directly proportional to the switching activity. This makes LM structure suitable for low-activity low-power applications. Double-edge triggered flip-flops examined here, have smaller power consumption for low input activity than single-edge flip-flops. It is found that, due to the specific design, TGFF internal activity follows the input activity (i.e. when the input is quiet, the voltages at the internal nodes of TGFF are constant and the internal activity is only due to the clock delay chain, Fig. 4).

TSPC, on the other hand, has significant internal activity when input is quiet, similar to the single-edge pulsed latch-based precharge-evaluate flip-flops (e.g. SDFF, HLFF, see [8]). Double-edge TSPC power consumptions for two cases of zero activity (D=0 and D=1) is similar due to the existence of two sub-circuits (for rising and falling clock edge capture), exactly one of which is active for each input level. Power consumption for zero input activity of double-edge TSPC is roughly half of that of single-edge TSPC for D=0.

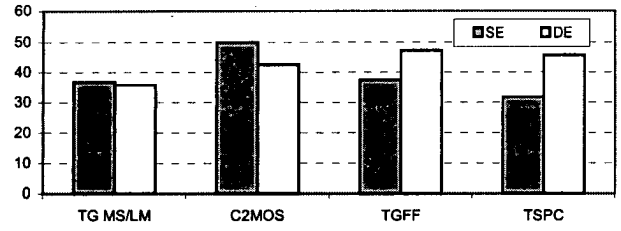

Fig. 8. EDP comparison for 50% data activity. EDP in fJ/500MHz for single-edge and fJ/250MHz for double-edge triggered storage elements

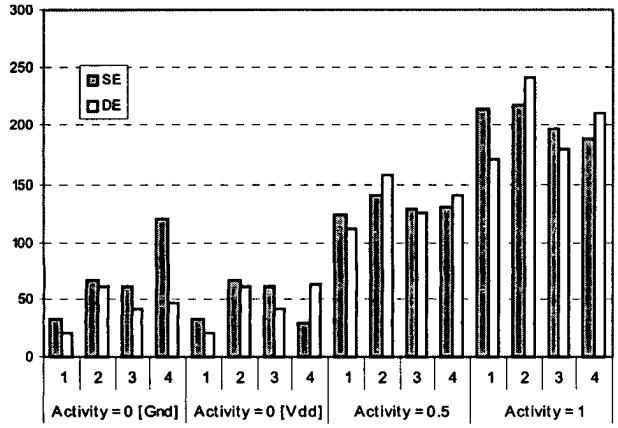

Fig. 9. Power consumption vs. data activity (power in μW). 1-TGMS/LM, 2-C^{2}MOS, 3-TGFF, 4-TSPC

5. CONCLUSION

A set of representative double-edge triggered storage elements is compared to the corresponding single-edge triggered storage elements in terms of EDP, delay and power consumption. It is found that Latch-Mux based structures perform better then their direct single-edge counterparts, due to shorter critical path and only slight increase in circuit complexity. Double-edge triggered flip-flops examined here, suffer performance degradation when compared to their single-edge counterparts, due to more complex design and the fact that most of the complexity increase affects the signal propagation along the critical path.

6. REFERENCES

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Table 1. Overall Performance Comparison

SETFF's	t_{su} [ps]		t_D [ps]		P_I [uW]	P_{CLK} [uW]	P_{TOT} [uW]	*EDP* [fJ/500MHz]
TGMS	160		300		80.0	32.1	123.2	36.9
C^{2}MOS	100		354		110.8	27.5	141.1	49.9
TGFF	50		292		110.5	8.7	128.5	37.5
TSPC	80		254		97.8	30.1	130.7	31.7
DETFF's	$t_{su,r}$ [ps]	$t_{su,f}$ [ps]	t_{D1} [ps]	t_{D2} [ps]	P_I [uW]	P_{CLK} [uW]	P_{TOT} [uW]	*EDP* [fJ/250MHz]
TGLM	120	115	322	322	83.3	20.5	111.6	35.9
C^{2}MOS	58	52	266	268	122.9	27.3	158.3	42.5
TGFF	93	68	372	374	104.7	7.8	125.7	47.1
TSPC	74	82	319	329	115.4	19.8	140.3	45.5