Dynamic Flip-Flop with Improved Power

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Abstract

An improved design of a dynamic Flip-Flop is presented. Proposed design overcomes the problem of the glitch at the output and improves Power-Delay Product for about 10%, while preserving logic embedding property. This is accomplished by equalizing the t_{pLH} and t_{pHL} of the flip-flop and careful design of keeper elements in the circuit. New design introduces insignificant area increase.

1. Introduction

Semi-Dynamic Flip-Flop [1] has been used in high-performance applications because of its small delay, logic embedding feature and simple topology. It is considered to be one of fastest flip-flops today. Good performance of this circuit is achieved by use of precharging on internal node (X on Figure 1) and removing low-to-high transitions from critical path, ending with only one single-transistor path at the output (M_{p2}). Moreover, structure of the flip-flop allows large amount of preceding logic to be collapsed into flip-flop circuitry with no or very small penalty in number of transistors and performance, thus significantly reducing both critical path in the system and the chip area. This favourable property (logic-embedding) is readily observed by noting that arbitrary non-inverting logic can replace transistor M_{n2} in Figure 1, which is functionally equivalent to capturing the output of externally placed logic.

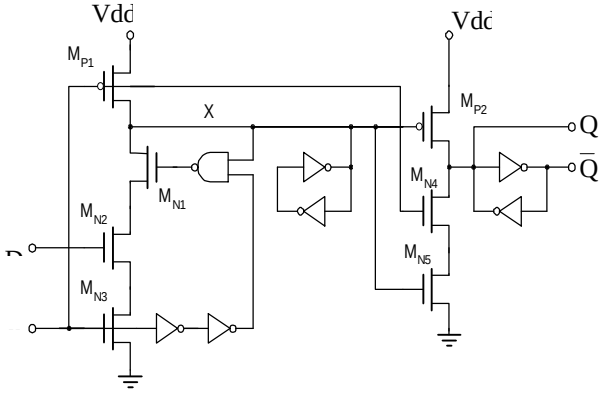


Figure 1. Semi-Dynamic Flip-Flop

However, SDFF is not suitable for applications where low power is required since its power consumption limits its utilization. It is noticed that considerable portion of power dissipated in SDFF occurs due to unnecessary and false transitions that result in glitches generally increasing the power consumed by consecutive logic as well.

2. SDFF Operation

SDFF operation falls into the category of pulsed hybrid latch approach introduced by Partovi [2]. The locking mechanism defines short period of time following active clock edge during which a change is allowed. Semi-Dynamic Flip-Flop is transparent during time window determined by the delay through two inverters and NAND gate (Fig.1). If input is at high logic level during that period, internal signal X will fall, which forces output to high level. If the flip-flop input is zero during the transparency time, there will be no other opportunity for internal signal to fall, and high level is used to force the output to low level.

Essentially, there are two separate mechanisms for latching logical zero and logical one. The mechanism for capturing logical zero is default one, and is masked by the input conditions for capturing logical one (input at high logic level immediately after rising edge of the clock). While this is the key for providing simplicity at the input, necessary for logic-embedding property, it can be also noticed that this ensures much smaller delay of the device for low than that for high logic level. This feature, however, causes a "static-one-hazard" at the output when both D and Q are ones, which is a major problem of this topology. This glitch results also in an unnecessary additional power consumption of consecutive logic.

Another important issue, is the use of the keepers. The keeper is used to hold the value of a dynamic node that would otherwise be in high impedance and therefore sensitive to leakage current effects and noise, especially in low-power applications where clock gating techniques are usually employed. This simple method has some disadvantages as well: in order to change the state of SDFF, two keepers have to be overpowered, which introduces another portion of unnecessary power consumption and increase in the delay. In addition, the keeper at the output is particularly troublesome for certain applications where the flip-flop has to have certain driving capability during the entire clock period. For example, pass-transistor logic with pass-inputs driven by flip-flop requires strong driving after its control signals change, which, in general, can happen during the time where it is only keeper who holds the value at the flip-flop output. This problem in SDFF structure can be overcame only by increasing size of the inverter in the keeper that drives the output. However, increase of the size of that inverter would severely degrade performance of the device during its own switching and is very limited by the functionality requirements.

3. Improvements and Optimization

Conditional capture techniques can generally be utilized if the goal is to minimize the power consumption. The idea of the conditional capture is to inhibit the transition of internal signal if this is not needed, i.e. if the output is already at the level that is to be set by the input signal. Unfortunately, application of this approach in SDFF topology requires excessive hardware overhead in the second stage, which would consume the power saved. Moreover, this requires including the input D into the second stage, which seriously degrades highly desirable logic embedding property of SDFF.

Another approach is to allow transitions on internal signal but disable its effect on the output until the correct value is set. This can be accomplished by delaying the control signal for resetting the output (Fig. 2). The sizes of the transistors that equalize high-to-low and low-to-high delays are chosen.

Considering the minimization of negative effect of keepers, careful analysis shows that both low-to-high and high-to-low transitions clash can be avoided on both nodes restored by the keeper in SDFF. Internal signal (X) needs to be restored only if clock is at the high logic level - more precisely, while this part of the circuit is not in the precharge phase, and evaluation is stopped with the end of transparency window. Use of delayed clock for the activation of the pull-up keeper allows setting the value of internal signal when keeper is inactive, avoiding the clash between pull-down and pull-up network, which increases the speed of the transition and reduces the power consumed. Pull-down keeping function can be associated with clock signal without any collision hazard. It is convenient to use existing transistor controlled by clock signal for this function, reducing number of transistors and reducing clock load.

In contrast, output keeper should turn on only when the clock is on low level. Again, delayed clock signals, generated for other purposes and available with no cost, are used to control the keeping function and to eliminate the possibility of clash at the output node. Note that it is also possible to associate keeping output at the low level with signal X, since this signal is used to preset the output (M_{p2}).

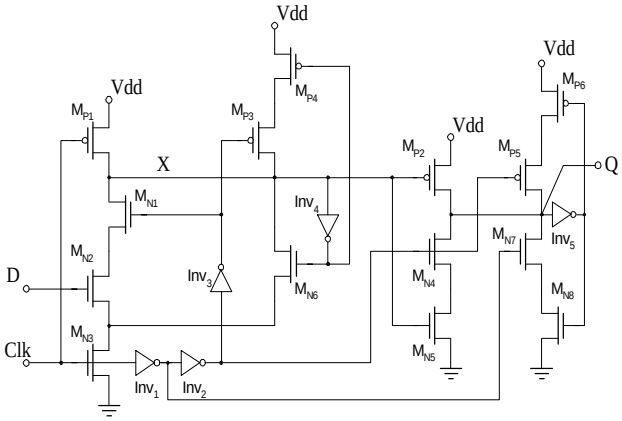


Figure 2. Proposed Flip-Flop

This design requires active levels of the control signals (high level on X and delayed clock) not to overlap unless needed by functionality. There is a possible hazardous situation that should be discussed: after the clock makes transition to zero, it is not clear which of control signals of second stage will first change its state and, theoretically, there is a possibility that output Q be for a short time erroneously connected to ground. However, the only transistor that drives internal signal is M_{P1}, which is small, owing to the fact that there is no classical keeper on the node and that the capacitance on the node X is considerable, that delay is much bigger than the two inverters delay: and therefore presenting no danger for the proper operation of the flip-flop. The behavior observed in the simulations strongly supports this argument.

4. Results

Proposed flip-flop is simulated, optimized and compared to SDFF using 0.25μ *Leff* CMOS technology with the supply voltage of 2.5V and the load of 14 minimal inverters in the same technology. The methodology of the optimization is similar to that in [3]. The criterions for the optimization are data-to-output delay and total power consumption of the circuit, clock driver and data driver, as elaborated in [3]. The power consumption is measured for highest data activity

(change once per clock period), which can always be subject to argument, since it is not always the parameter of interest and different structures exhibit considerably discrepant behavior for different data activities. In this particular case, however, similar structures and dynamic behaviors of these two flip-flops assure that this parameter is a good basis for comparison.

In addition to removing unwanted glitch at the output that could impair the performance of consecutive logic and introducing the keeper that can serve as a strong driving circuit, this flip-flop exhibits about 10% better performance in terms of PDP at the negligible expense in number of transistors and area compared to SDFF.

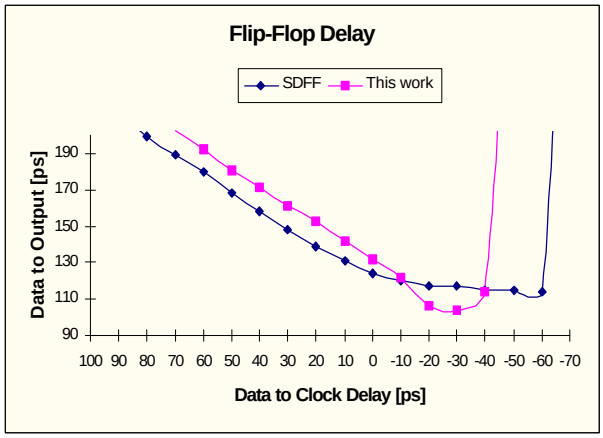


Figure 3. Delay Comparison

Figure 3 shows data-to-output delay characteristics of SDFF and proposed flip-flop. It can be seen that despite smaller absolute value of optimal set-up time, total delay of new structure is less than that of SDFF by about 8%.

The power consumptions comparison is presented in Figure 4. It can be observed that power consumption saving of the new structure has two components:

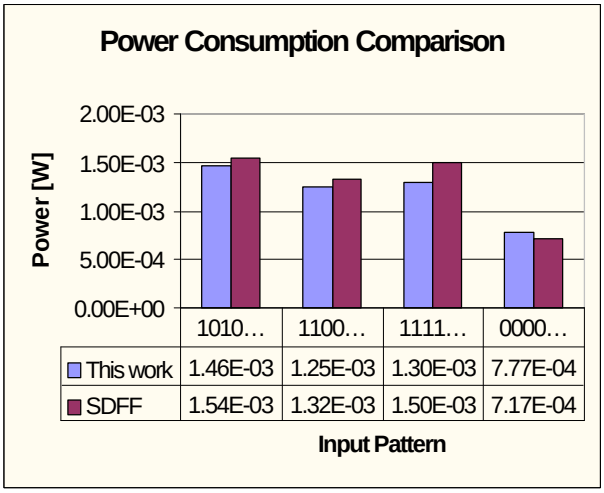
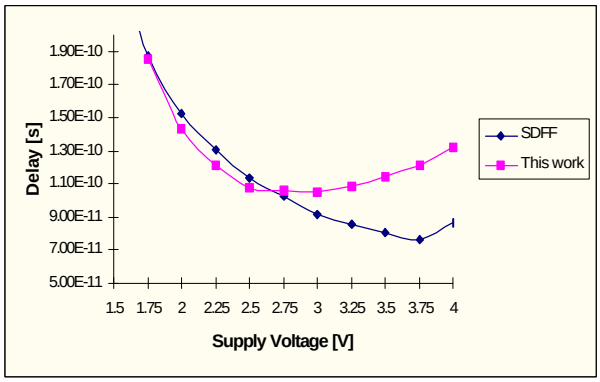


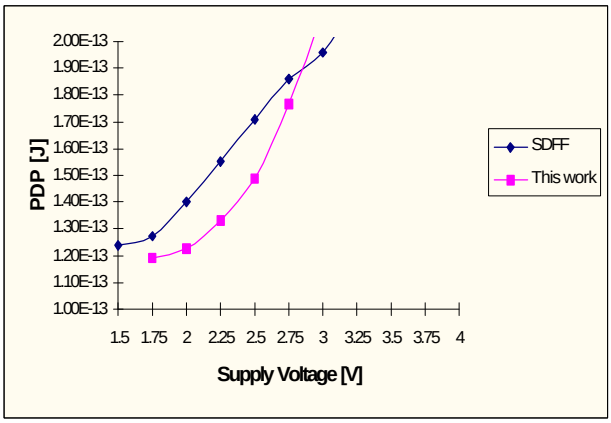
Figure 4. Power Consumption Comparison

- First component is due to less power consumed in overpowering the keepers in switching both internal node X and output Q. This component is visible in the difference between these two structures for highest input data activity (sequence 10101010...)
- Second component is saving due to elimination of the glitch at the output caused by static-one hazard, as stated above. This component becomes more visible as percentage of consecutive ones in input pattern increases, which can be observed for sequences 11001100... and 11111111...

Finally, the difference between power consumptions for input sequence 0000... in favor of SDFF shows higher consumption of new flip-flop's clock inverters when no other change in the circuit occurs. This effect, present with pattern 11001100... as well, but masked by dominant power saving accomplished by glitch elimination, can be explained by significantly higher load of these inverters as compared to SDFF. Having in mind that these values are much smaller than those obtained using other patterns, it can be stated that this difference has small importance to the performance of



a) Delay vs. Supply Voltage



b) PDP vs. Supply Voltage

Figure 5. Performance of Flip-Flops with Scaled Voltage Supply

the circuit.

Figure 5 shows behavior of both proposed flip-flop and SDFF when the supply voltages is scaled down. It must be noted that results are obtained using the transistor widths optimized for nominal supply voltage (2.5V). This means that results are not optimal for considerably different voltage supplies. However, the changes that would be obtained are believed to be in the same direction and for similar amount, in which case valid comparison basis is provided.

The new flip-flop shows improved characteristics over SDFF as supply voltage continues to decrease, as presented in Figure 5. The most valuable component of new circuit's performance improvement over SDFF is power consumption saving, due to excessive power reduction with supply voltage decrease and increase of its relative effect to the overall performance.

5. Conclusion

An improved design of Semi-Dynamic Flip-Flop is presented that eliminates unnecessary glitch at the output and that introduces conditional keeping function, avoiding clashes in transitions at critical nodes. This circuit outperforms earlier published structure for about 10% in terms of Power-Delay-Product while preserving desirable logic-embedding property. New design introduces negligible area increase and shows favorable characteristics as power supply scales down as compared to previous one.

6. References

[1] F. Klass, “Semi-Dynamic and Dynamic Flip-Flops with Embedded Logic,” *Symp. on VLSI Circ, Digest of Technical Papers*, June 1998

[2] H. Partovi, et. al., "Flow-Through Latch and Edge-Triggered Flip-Flop Hybrid Elements," *ISSCC Digest of Technical Papers*, February 1996

[3] V. Stojanovic, V. G. Oklobdzija, "Comparative Analysis of Master-Slave Latches and Flip-Flops for High-Performance and Low-Power Systems ", *IEEE Journal of Solid-State Circuits*, April 1999.

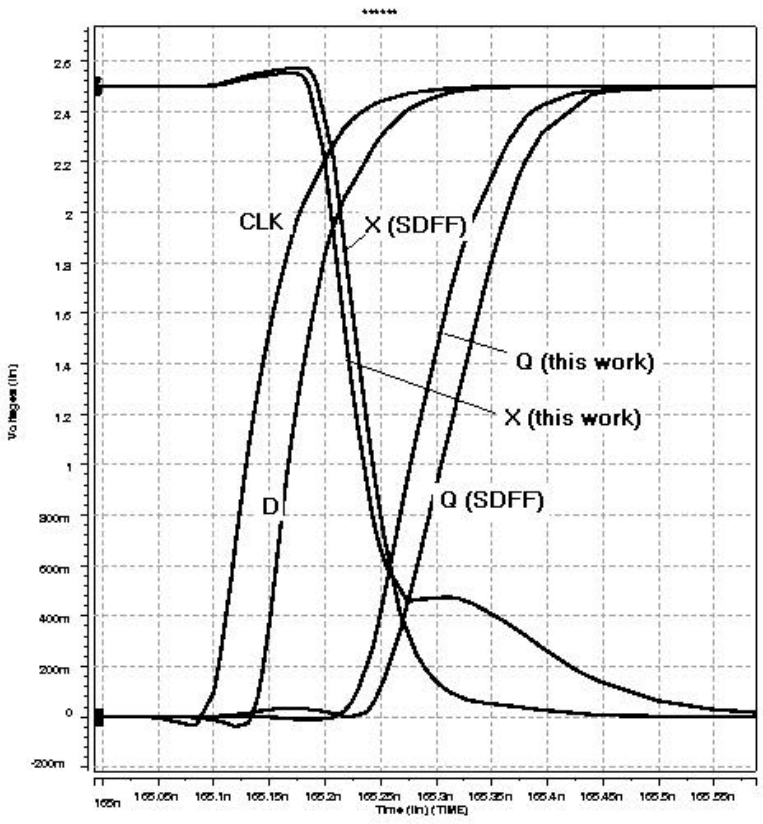


Figure 6. Typical Waveforms