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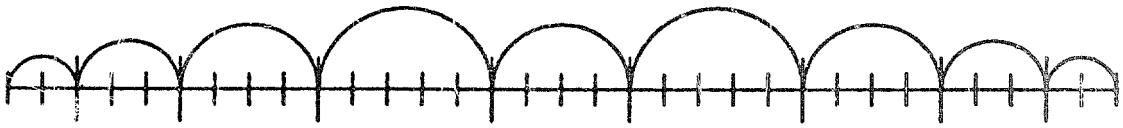
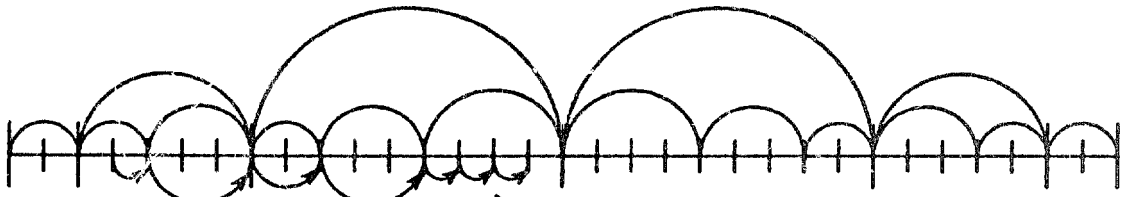
NEW MULTILEVEL SCHEME FOR FAST CARRY-SKIP ADDITION



(a) N=32, Δ=9

FIG.1



(b) N=32, Δ=7

A method is described which provides a way to achieve a fast addition of two binary numbers by using a multilevel carry-skip scheme optimally divided to attain speed comparable to carry-lookahead yet much simpler to implement and convenient for VLSI implementation. This multilevel carry-skip addition scheme, with the optimized division into the carry-skip groups, achieves speed comparable to the carry-lookahead scheme. Yet, this scheme is much simpler than carry-lookahead to implement and is uniform in fan-in and fan-out requirements. Therefore, it is very convenient for VLSI implementations, and we claim that it makes much more sense for VLSI than carry-lookahead scheme.

In certain fast carry-skip adders, the speed is achieved by dividing the carry chain into groups of bits over which carry signals could skip. The sizes of the groups are chosen to minimize the maximum delay that a carry signal can experience. The following shows that further significant increases in speed can be achieved by dividing the groups of bits into blocks and giving carry signals the ability to skip over blocks, as well as groups. Moreover, how to choose the group and block sizes optimally to minimize the maximum delay of a signal will be set forth.

The following example shows how it is possible to increase the speed of the adder by allowing signals to skip over blocks of bits.

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FIG.2

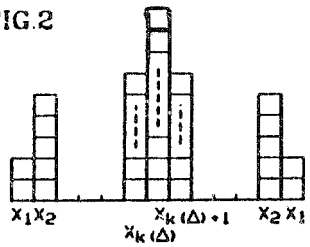

FIG.3

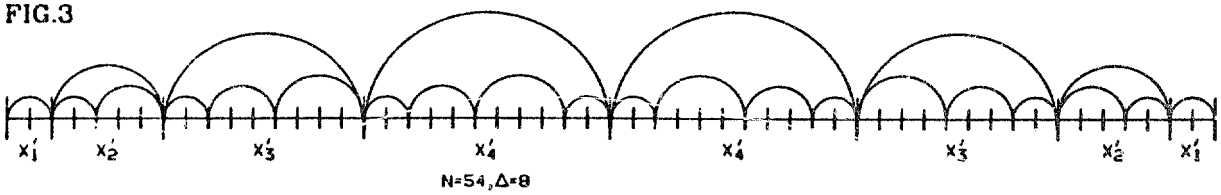

Fig. 1a shows a carry chain of length 32 divided optimally into groups by a predetermined algorithm. The maximum delay of a carry signal is 9 units. Fig. 1b shows the same chain with the bits divided optimally into groups and blocks. The maximum delay is now 7 units. This increase in speed can be achieved with a very small increase in the number of transistors used to build the adder.

The statement of the algorithm for dividing the carry chain into groups and blocks is as follows.

Let N denote the number of bits in the adder.

Define $Y_i = i + 1/2i + 1/4i^2 + 1/8(1-(-1)^i)$, $i = 1,2\ldots$. For each positive integer M define $k(m) = 1/2m - 1/4(1-(-1)^m)$. $2k(m)$ is the largest integer $\leq m$.

Step 1. Define Δ to be the smallest positive integer such that

$$N \leq 2\sum_{i=1}^{k(\Delta)} Y_i + \frac{1}{2}(1-(-1)^{\Delta})\, Y_{k(\Delta)+1}.$$

Step 2. Given Δ and $Y_1, Y_2, \ldots, Y_{k(\Delta)+1}$, construct the symmetric array of squares shown in Fig. 2. There are Δ columns in this figure, and the i-th column contains Y_i squares,

$i = 1,\ldots,k(\Delta),k(\Delta) + 1/2\ (1-(-1)^{\Delta})$.

Step 3. By definition of Δ, the array contains at least N squares. Beginning with the first row in the array, shade in squares, row by row, until N squares are shaded in. Let X_i denote the number of

shaded squares in column i, i=1,..., Δ. Divide the carry chain into Δ blocks of sizes $X_1,\ldots, X_\Delta$, respectively.

Step 4. Divide the i-th block into $\Delta_i = [(2\sqrt{X_i + 5/4} - 2)]$ groups as follows. ([R] denotes the greatest integer $\leq$ R.)

Let $y_{ij} = \min\{1 + j, 2 + \Delta_i - j\}$, $j = 1,\ldots, \Delta_i$. Construct a symmetric figure, similar to Fig. 2, containing Δ_i columns with y_{ij} squares in column j. This figure will contain at least X_i squares. Shade in X_i squares, row by row, starting with the first row. Let X_{ij} denote the number of shaded squares in the j-th column. Divide the i-th block of the carry chain into Δ_i groups with x_{ij} being the size of the j-th group, $j = 1,\ldots,\Delta_i$.

It can be verified that the minimum delay of a carry signal in a carry chain, divided into blocks of groups of bits by the procedure just described, is Δ.

Example. Consider the optimal division of a 54-bit carry chain. This results in

$$Y_1 = 2,\ Y_2 = 4,\ Y_3 = 7,\ Y_4 = 10,\ Y_5 = 14,\ldots .$$

since

$$54 \leq 2(Y_1 + Y_2 + Y_3 + Y_4) + Y_5 = 60$$

we have $\Delta = 9$. It follows that

$$X_1 = X_9 = 2,\ X_2 = X_8 = 4,\ X_3 = X_7 = 7,\ X_4 = 10,\ X_5 = X_6 = 9.$$

and

$$\Delta_1 = \Delta_9 = 1,\ \Delta_2 = \Delta_8 = 2,\ \Delta_3 = \Delta_7 = 3,\ \Delta_4 = \Delta_5 = \Delta_6 = 4.$$

The sizes of the groups in blocks 1,2,3,4, and 5 are given by

$$x_{11} = 2,$$

$$x_{21} = x_{22} = 2,$$

$$x_{31} = x_{33} = 2,\ x_{32} = 3,$$

$$x_{41} = x_{44} = 2,\ x_{42} = x_{43} = 3,$$

$$x_{51} = x_{53} = x_{54} = 2,\ x_{52} = 3,$$

respectively. The optinal carry chain is shown in Fig. 3. The maximum delay of a carry signal in this chain is $\Delta = 9$.