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NEW CONFIGURATION OF CMOS-DOMINO LOGIC

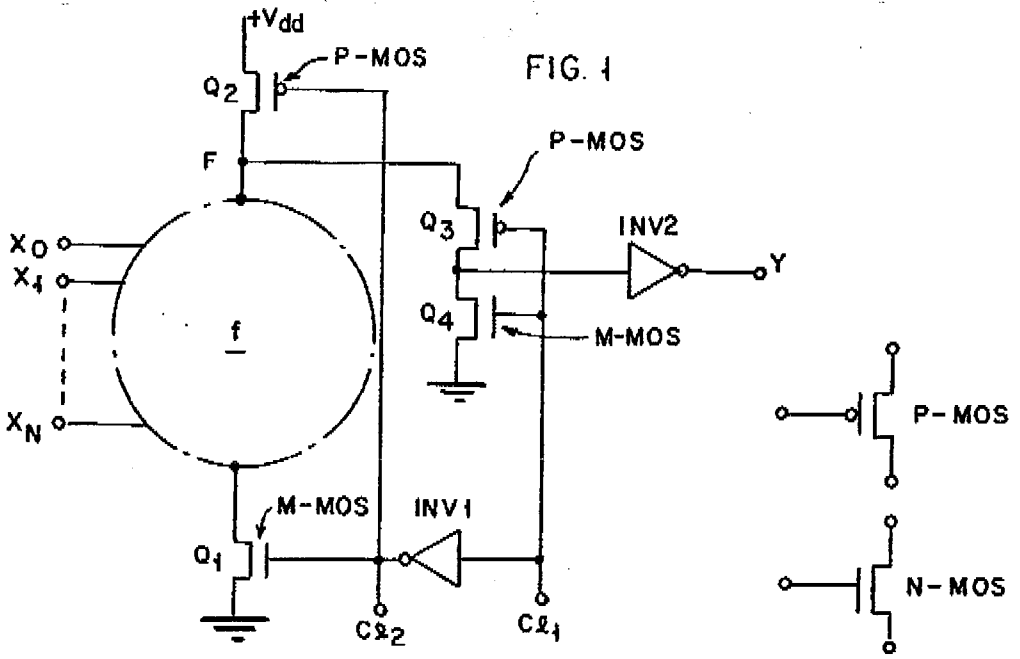


FIG. 1

This article describes a circuit configuration that has all of the advantages of a CMOS-DOMINO circuit family, yet it assures consistent precharge and is "glitch-free".

The structure to be used as a CMOS-DOMINO logic block has all of the advantages of CMOS-DOMINO logic as described in [*]. The function of this logic complies with all restrictions imposed on CMOS-DOMINO (no inversion possible) and has all the benefits of this logic: CMOS power requirements and speed of dynamic n-MOS logic.

However, this logic family is "glitch-free", i.e., functional block f is fully precharged during each precharge period so that during the "evaluation" phase the node F (Fig. 1) cannot swing from "1" to "0" due to the redistribution of charge (as in CMOS-DOMINO logic) or swing from "1" to "0" and back to "1" (glitch) as in the CVS logic family. All of this causes the wrong value to be propagated through the logic network to the primary output(s).

NEW CONFIGURATION OF CMOS-DOMINO LOGIC - Continued

FIG. 2

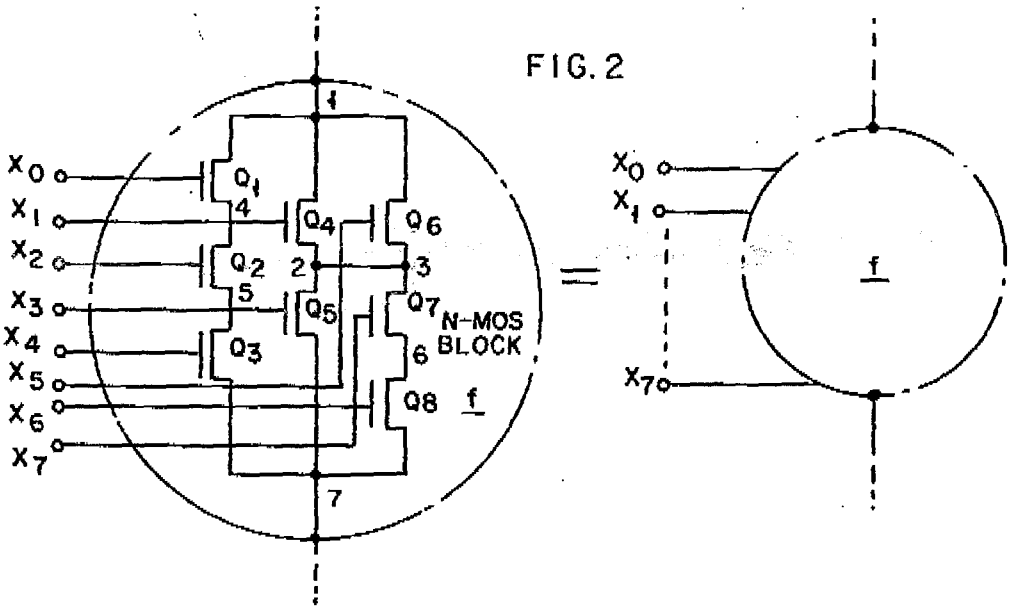
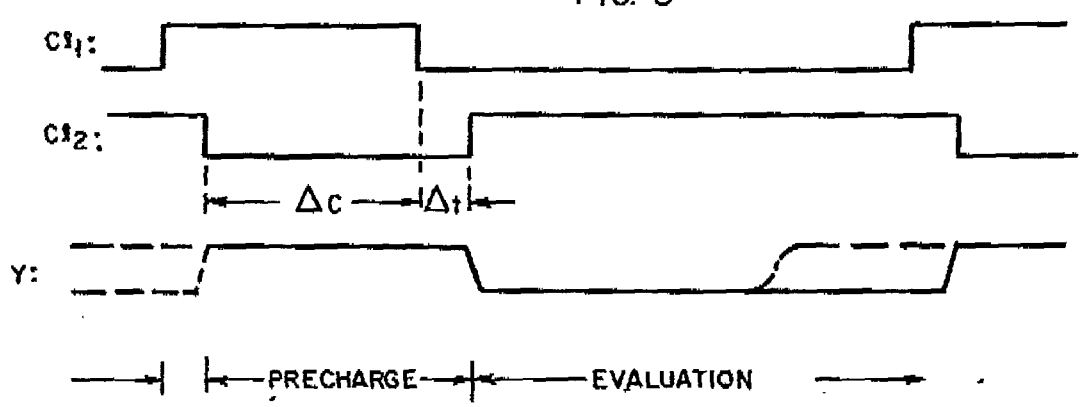


FIG. 3



The logic also works in two phases: "Precharge" - when all the internal nodes in the functional block f are precharged to "1" logic value; "evaluation" - when the selected blocks are discharged, due to the logic value of the inputs, and this change is propagated through the logic network in a "DOMINO" fashion.

There are two separate clocks applied, Cl_1 and Cl_2 (see Fig. 1 and timing diagram Fig. 3). The clock Cl_2 is phase shifted relative to the clock Cl_1 which is easily achieved by passing clock Cl_1 through the inverter INV_1 (Fig. 1). This can be done "locally" at each block (as in Fig. 1), or clocks Cl_1 and Cl_2 can be generated at one place and distributed throughout the chip assuring that there is no "clock skew" between clocks Cl_1 and Cl_2.

NEW CONFIGURATION OF CMOS-DOMINO LOGIC - Continued

The feature of this logic is that during the interval Δ C (Fig. 3), all the outputs Y (Fig. 1), which are inputs into the subsequent blocks, are made logic "1", which means that all the transistors $Q_1 \ldots Q_8$ (Fig. 2) in the functional block f are made conducting ("on"). That means that all of the paths in f are open during "precharge" which in turn assures that all the internal nodes 1,2,3.. ,7 with associated capacitances are charged to logic "1".

This feature assures a complete precharge of the blocks and provides for a safe "glitch-free" operation of this type of logic. Further advantages of the circuit configuration include simplicity and simple clock requirements.

Reference

[*] R. H. Krambeck, C. M. Lee, H. S. Law, "High-Speed Compact Circuits with CMOS," IEEE Jo. of SSC SC-17, (June 1982).