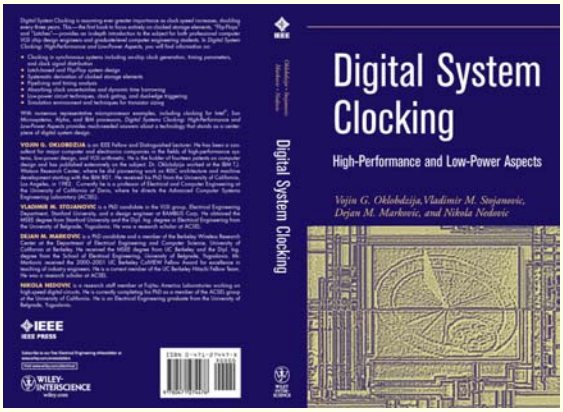
Digital System Clocking:

High-Performance and Low-Power Aspects

Vojin G. Oklobdzija, Vladimir M. Stojanovic, Dejan M. Markovic, Nikola M. Nedovic

Chapter 9: Microprocessor Examples



Wiley-Interscience and IEEE Press, January 2003

Microprocessor Examples

- Clocking for Intel® Microprocessors
  - IA-32 Pentium® Pro
  - First IA-64 Microprocessor
  - Pentium 4
- Sun Microsystems UltraSPARC-III® Clocking
  - Clocking and CSEs
- Alpha® Clocking: A Historical Overview
  - Clocking and CSEs
- IBM® Microprocessors
  - Level-Sensitive Scan Design
  - Examples of CSEs

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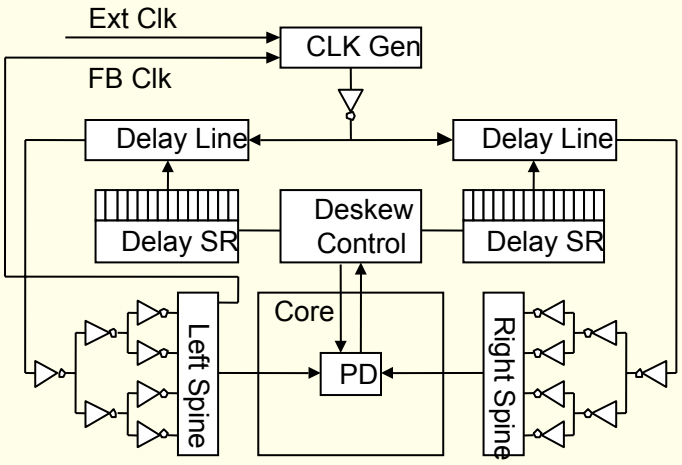
Intel® Microprocessor Features

	Pentium® II	Pentium® III	Pentium® 4
MPR Issue	June 1997	April 2000	Dec 2001
Clock Speed	266 MHz	1GHz	2GHz
Pipeline Stages	12/14	12/14	22/24
Transistors	7.5M	24M	42M
Cache (I/D/L2)	16k/16K/-	16K/16K/256K	12K/8K/256K
Die Size	203mm^2	106mm^2	217mm^2
IC Process	0.28µm, 4M	0.18µm, 6M	0.18µm, 6M
Max Power	27W	23W	67W

Source: Microprocessor Report Journal

IA-32 Pentium® Pro

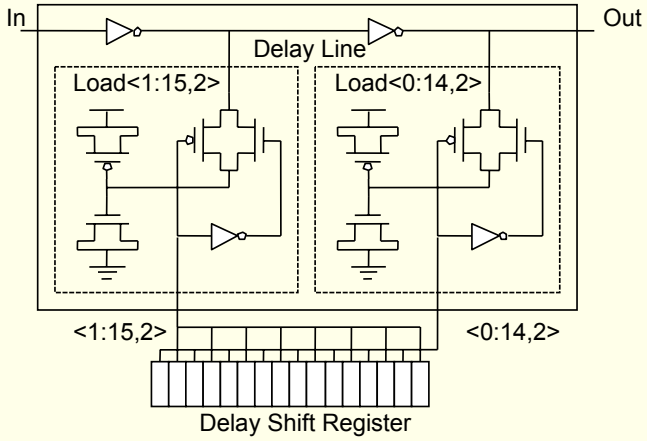


Clock distribution network with deskewing circuit (Geannopoulos and Dai 1998), Copyright © 1998 IEEE

Adaptive Deskewing Technique

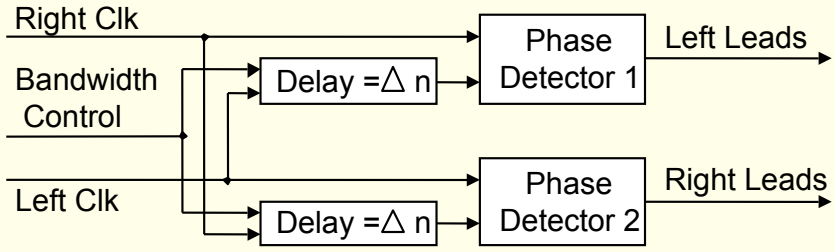
- Equalization of two clock distribution spines by compensating for delay mismatch
  - Delay lines
  - Phase detector
  - Controller
- Result: global clock skew of only 15ps
  - 0.25μm technology
  - 7.5M transistors

IA-32 Pentium® Pro



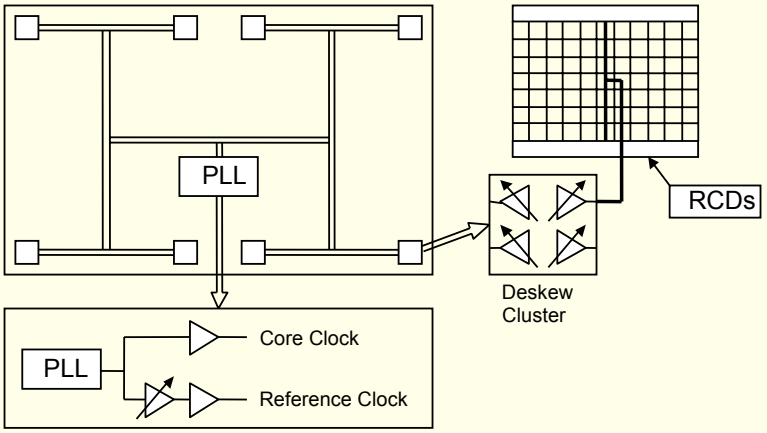
Delay shift register
(Geannopoulos and Dai 1998), Copyright © 1998 IEEE

IA-32 Pentium® Pro



Phase detector
(Geannopoulos and Dai 1998), Copyright © 1998 IEEE

First IA-64 Microprocessor

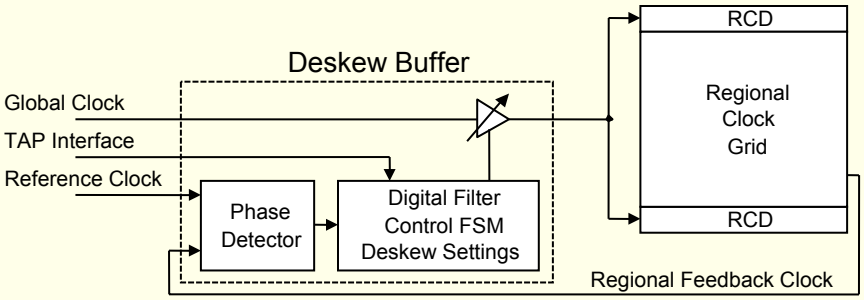


Clock distribution topology
(Rusu and Tam 2000), Copyright © 2000 IEEE

Programmable Deskew Units

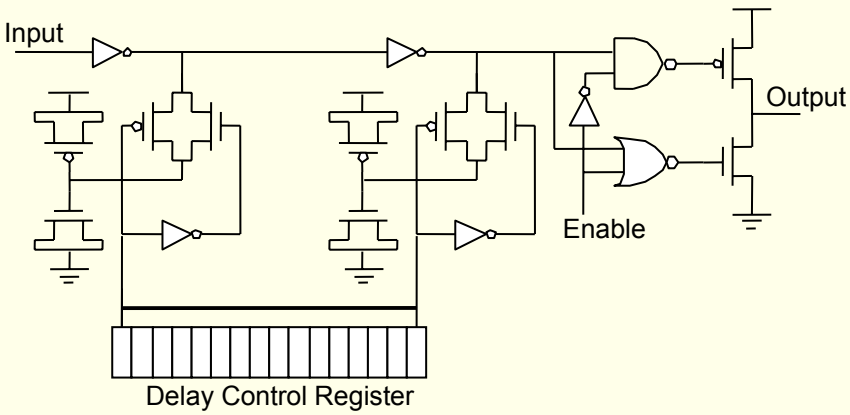
- Strategy similar to that in IA-32
- External differential clock
  - System bus frequency
- PLL generates internal clock
  - 2x frequency
- Clock distribution architecture
  - Balanced global clock tree
  - Multiple deskew buffers
  - Multiple local clock buffers

First IA-64 Microprocessor



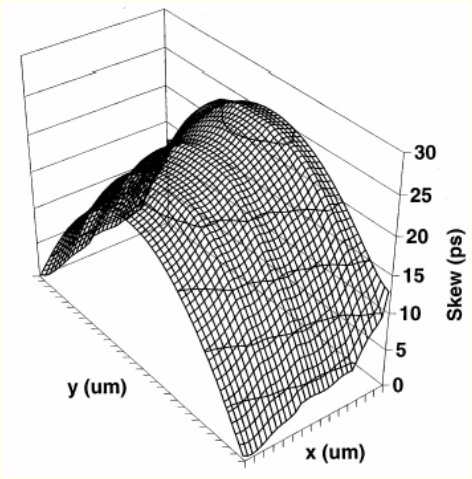
Deskew buffer architecture
(Rusu and Tam 2000), Copyright © 2000 IEEE

First IA-64 Microprocessor



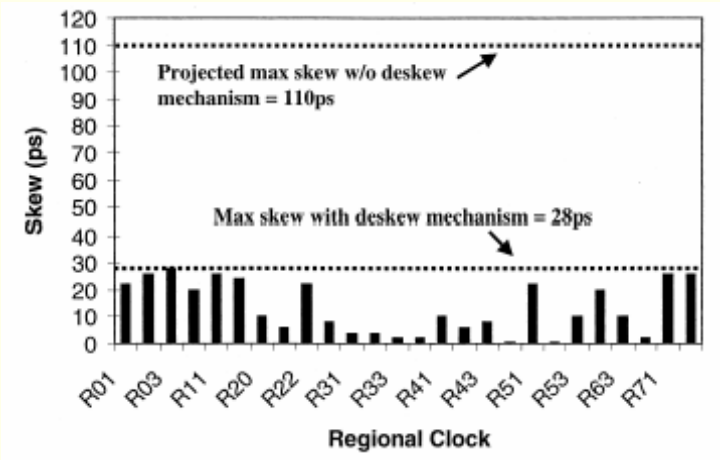
Digitally controlled delay line
(Rusu and Tam 2000), Copyright © 2000 IEEE

First IA-64 Microprocessor



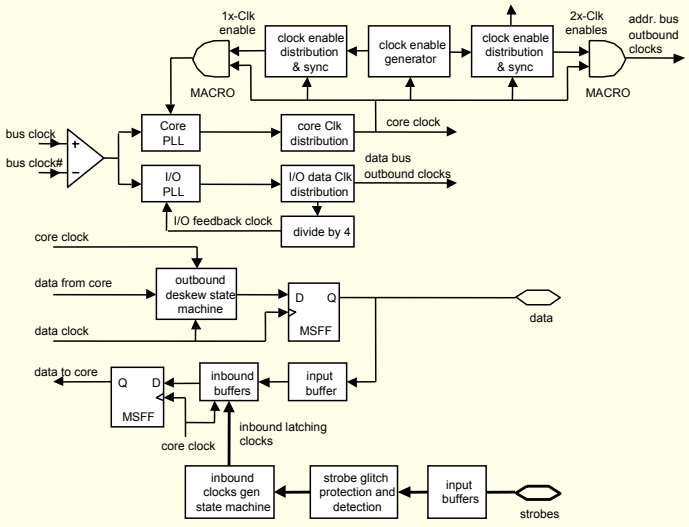
Simulated regional clock-grid skew
(Rusu and Tam 2000), Copyright © 2000 IEEE

First IA-64 Microprocessor



Measured regional clock skew
(Rusu and Tam 2000), Copyright © 2000 IEEE

Pentium® 4

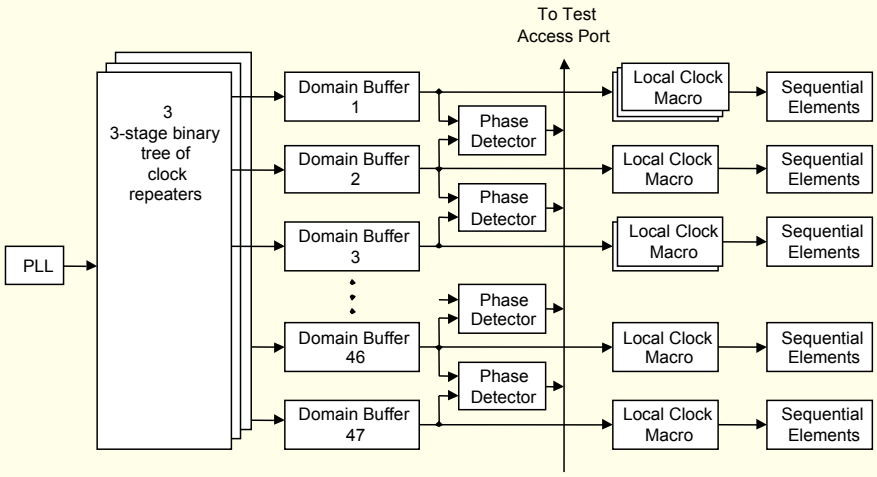


Core and I/O clock generation
(Kurd et al. 2001), Copyright © 2001 IEEE

Multi-GHz Clock Network in Pentium 4

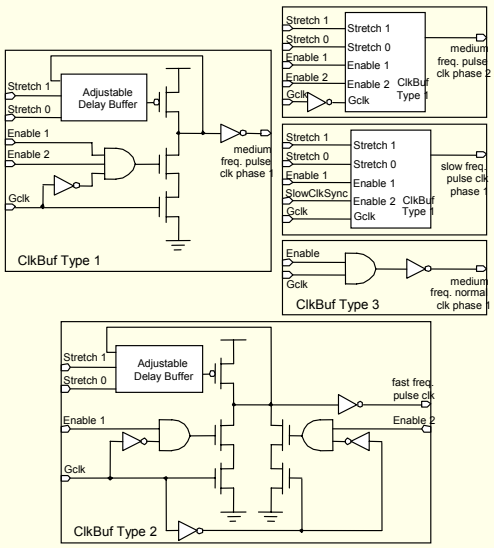
- Three core and three I/O frequencies (total 6 frequencies running concurrently)
- Differential off-chip reference clock
  - PLL synthesizes core and I/O clocks
- Global core clock distribution
  - 47 independent clock domains
  - Each domain has 5-bit deskew control register
- Clock skew < 20ps

Pentium® 4



Logical diagram of core clock distribution
(Kurd et al. 2001), Copyright © 2001 IEEE

Pentium® 4



Example of local clock buffers generating various frequency, phase and types of clocks
(Kurd et al. 2001), Copyright © 2001 IEEE

Intel Clocking: Summary

- Increasing clock speeds and die size
  - Balancing the clock skew in large designs using simple RC trees is becoming less effective
- Insertion delay 7-8FO4 due to increased die
  - Comparable to the clock period
- Clock skew control has been getting harder to due to increased PVT variations
- Inductive effects at multi-GHz rates
- Use of active deskewing circuits

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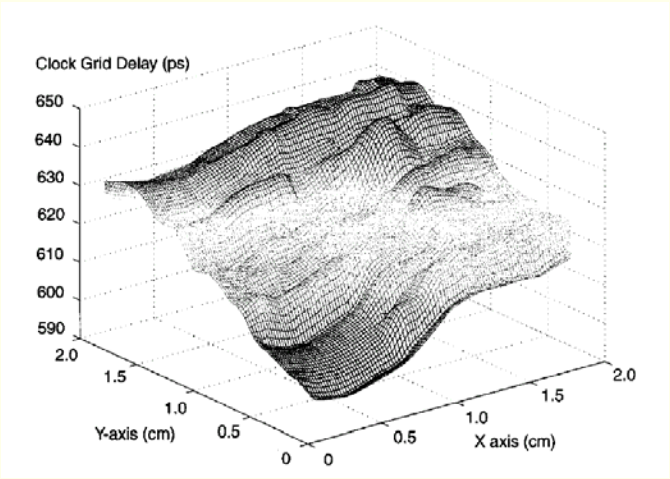
UltraSPARC® Family Characteristics

	UltraSPARC-I®	UltraSPARC-II®	UltraSPARC-III®
Year	1995	1997	2000
Architecture	SPARC V9, 4-issue	SPARC V9, 4-issue	SPARC V9, 4-issue
Die size	17.7x17.8mm^2	12.5x12.5mm^2	15x15.5mm^2
# of transistors	5.2M	5.4M	23M
Clock Frequency	167MHz	330MHz	1GHz
Supply voltage	3.3V	2.5V	1.6V
Process	0.5µm CMOS	0.35µm CMOS	0.15µm CMOS
Metal layers	4 (Al)	5 (Al)	7 (Al)
Power consumption	<30W	<30W	<80W

UltraSPARC-III: Clocking

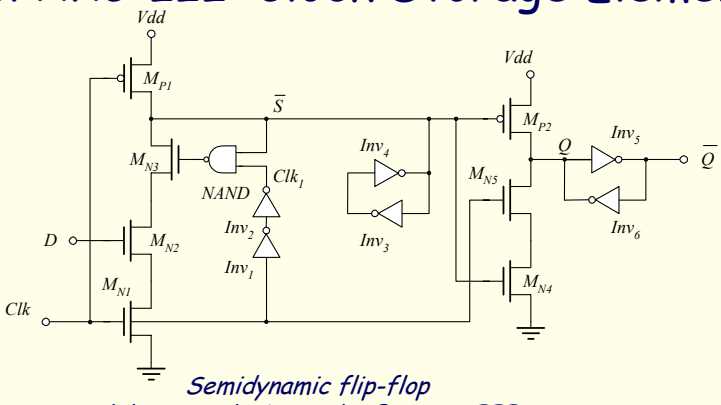
- Performance-driven high-power clock distribution
- Eight logic gates per cycle
- High-speed semi-dynamic flip-flops with logic embedding
- Large hold time mandates use of advanced tools for fixing fast-path violations

UltraSPARC-III®: Clocking



Clock distribution delay in UltraSPARC-III (Heald et al. 2000), Copyright © 2000 IEEE

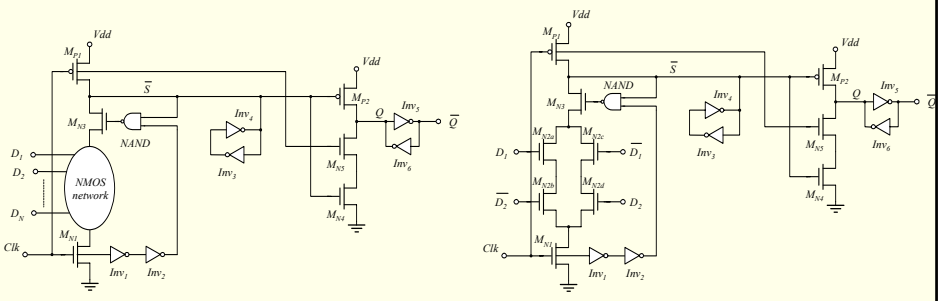
UltraSPARC-III: Clock Storage Elements



Semidynamic flip-flop (Klass 1998), Copyright © 1998 IEEE

- Single-ended dynamic structure with use of keepers for static operation and use of clock pulsing
- Positive feedback (NAND) improves low-to-high setup time
- Fast, at the price of high internal and clock power

UltraSPARC-III: Clock Storage Elements

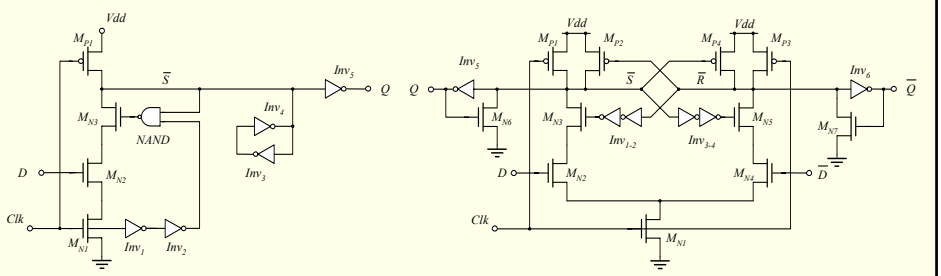


Logic embedding in a semi-dynamic flip-flop *Two-input XOR function*

(Klass, 1998), Copyright © 1998 IEEE

- A non-inverting logic function can be embedded by replacing the input D transistor with an n-MOS logic network
- Necessary for fitting 8 logic stages in cycle time, also used for scan
- Complexity of embedded logic limited by the n-MOS stack depth

UltraSPARC-III: Clock Storage Elements

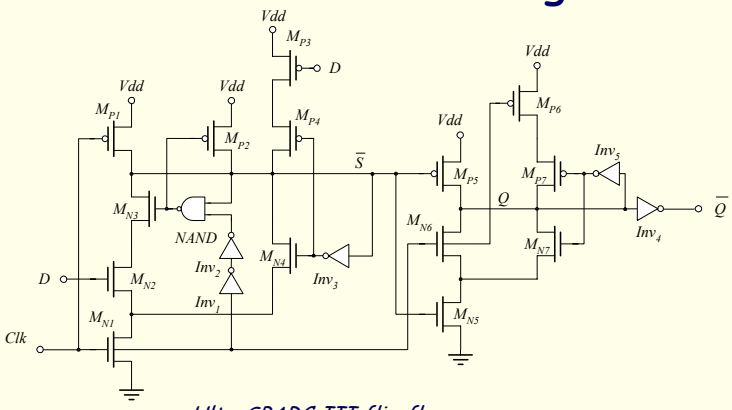


Single-ended dynamic SDFF *Differential dynamic SDFF*

(Klass, 1998), Copyright © 1998 IEEE

- Dynamic version of SDFF used in dynamic logic paths
- Outputs exercise precharge-evaluate sequence to ensure monotonicity

UltraSPARC-III: Clock Storage Elements



UltraSPARC-III flip-flop
(Heald et al. 2000), Copyright © 2000 IEEE

- Final UltraSPARC-III flip-flop modified by decoupling keepers to increase immunity to α-particles
- Somewhat degraded speed and logic embedding property

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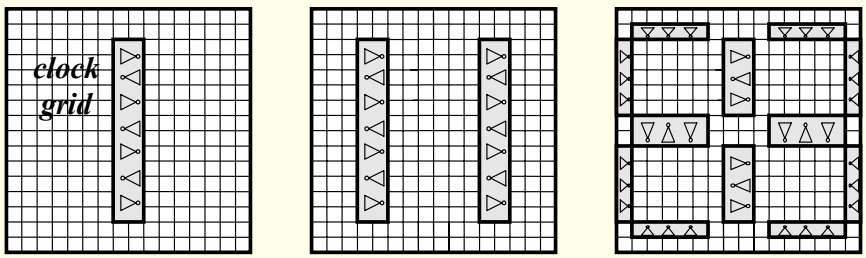
Alpha® Microprocessor Features

	21064	21164	21264	21364
# transistors [M]	1.68	9.3	15.2	152
Die Size [mm^2]	16.8x13.9	18.1x16.5	16.7x18.8	21.1x18.8
Process	0.75µm	0.5µm	0.35µm	0.18µm
Supply [V]	3.3	3.3	2.2	1.5
Power [W]	30	50	72	125
Clk Freq. [MHz]	200	300	600	1200
Gates/Cycle	16	14	12	12

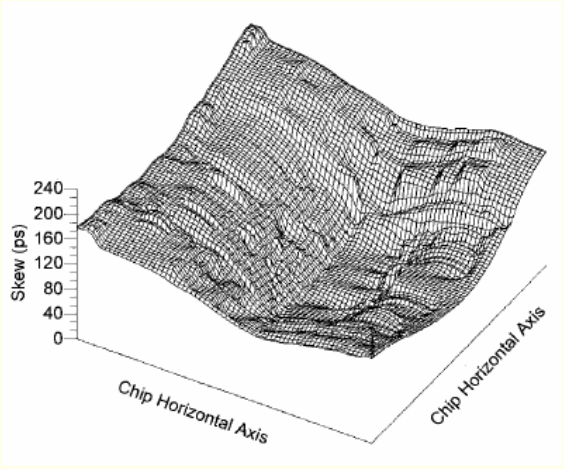
Alpha® Microprocessors: Clocking



(a) (b) (c)

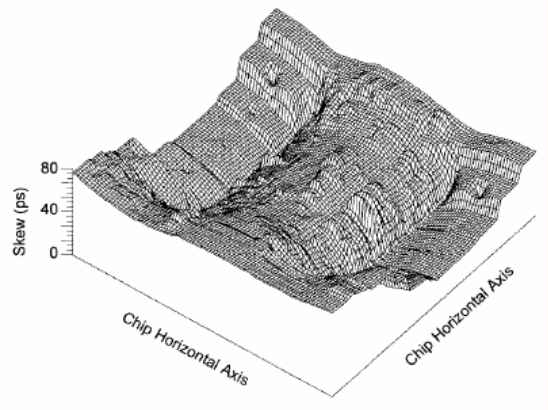
Alpha microprocessor final clock driver location:
(a) 21064, (b) 21164, (c) 21264

Alpha® Microprocessors: Clocking



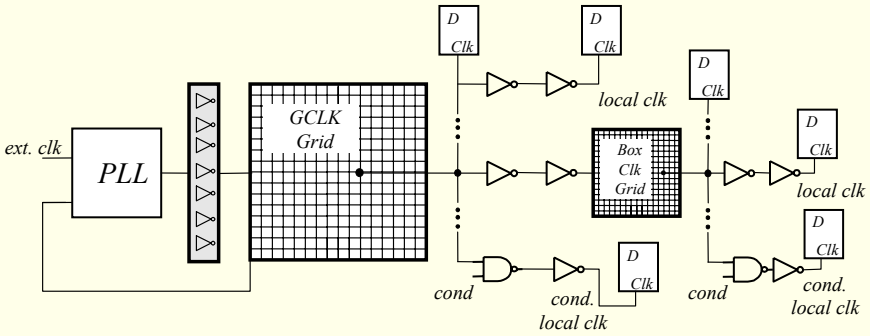
21064 clock skew
(Gronowski et al. 1998), Copyright © 1998 IEEE

Alpha® Microprocessors: Clocking



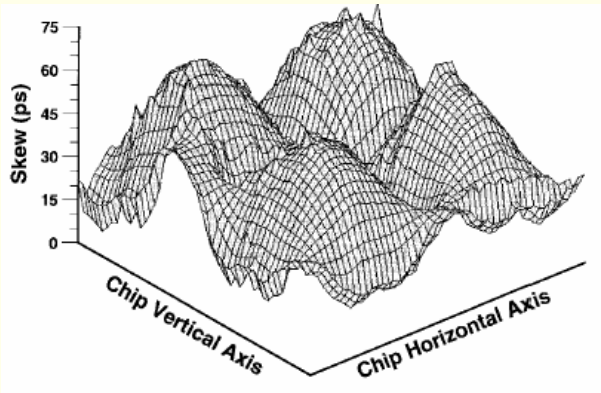
21164 clock skew
(Gronowski et al. 1998), Copyright © 1998 IEEE

Alpha® Microprocessors: Clocking



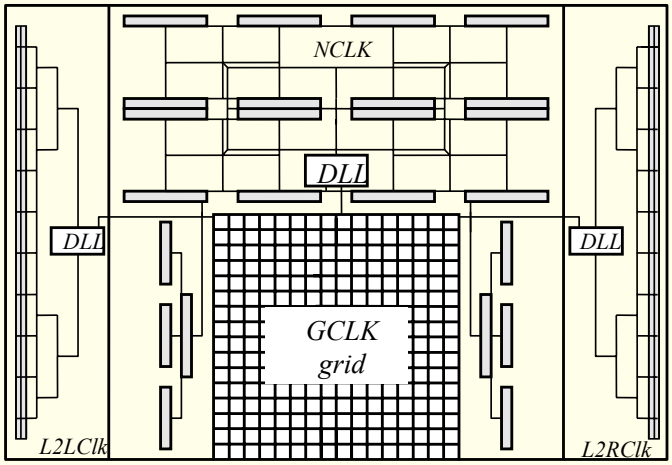
21264 clock hierarchy
(Gronowski et al. 1998), Copyright © 1998 IEEE

Alpha® Microprocessors: Clocking



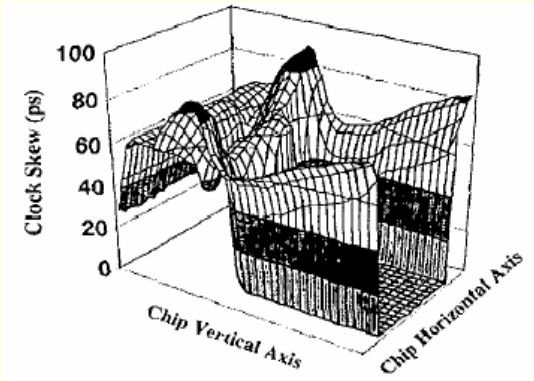
21264 clock skew
(Gronowski et al. 1998), Copyright © 1998 IEEE

Alpha® Microprocessors: Clocking



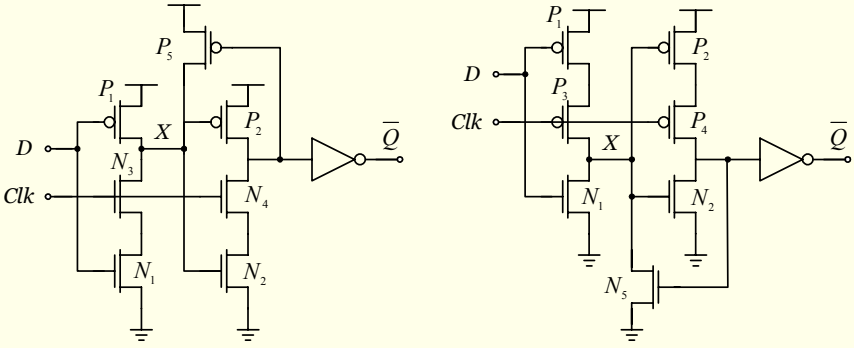
21364 major clock domains
(Xanthopoulos et al. 2001), Copyright © 2001

Alpha® Microprocessors: Clocking



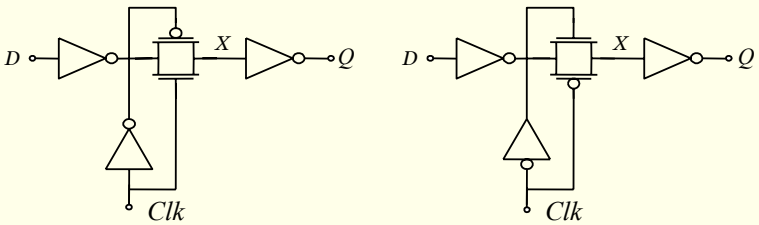
21364, NCLK clock skew
(Xanthopoulos et al. 2001), Copyright © 2001 IEEE

Alpha® µP: Clock Storage Elements



21064 modified TSPC latches
(Gronowski et al. 1998), Copyright © 1998

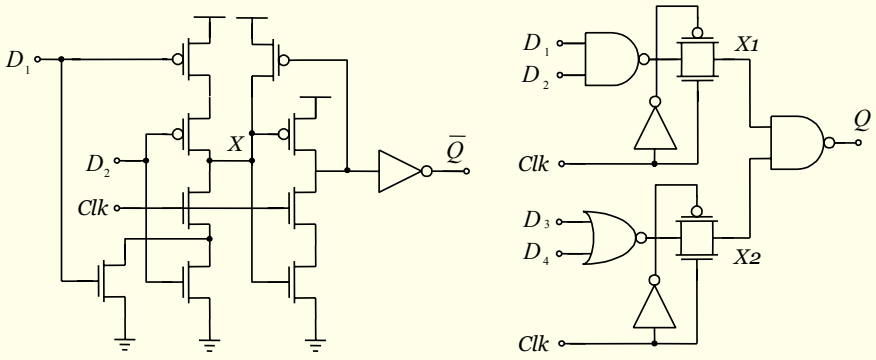
Alpha® µP: Clock Storage Elements



(a) (b)

21164: (a) phase-A latch, (b) phase-B latch
(Gronowski et al. 1998), Copyright © 1998 IEEE

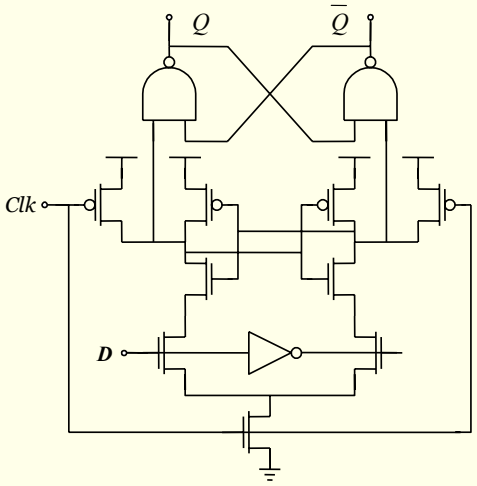
Alpha® µP: Clock Storage Elements



(a) (b)

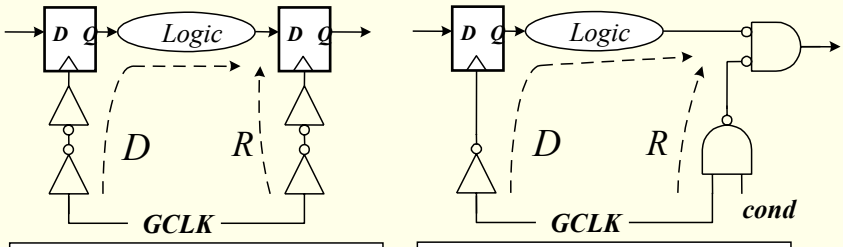
Embedding of logic into a latch:
(a) 21064 TSPC latch, one level of logic;
(b) 21164 latch, two levels of logic.
(Gronowski et al. 1998), Copyright © 1998 IEEE

Alpha® µP: Clock Storage Elements



21264 flip-flop
(Gronowski et al. 1998), Copyright © 1998 IEEE

Alpha® Microprocessors: Timing



Critical Path Definition and Criteria
- *Identify common clock, D and R*
- *Maximize D*
- *Minimize R*

$$D+U-R \leq T_{cycle}$$

Race Definition and Criteria
- *Identify common clock, D and R*
- *Minimize D*
- *Maximize R*

$$D \geq R+H$$

Critical-path and race analysis for clock buffering and conditioning (Gronowski et al. 1998), Copyright © 1998 IEEE

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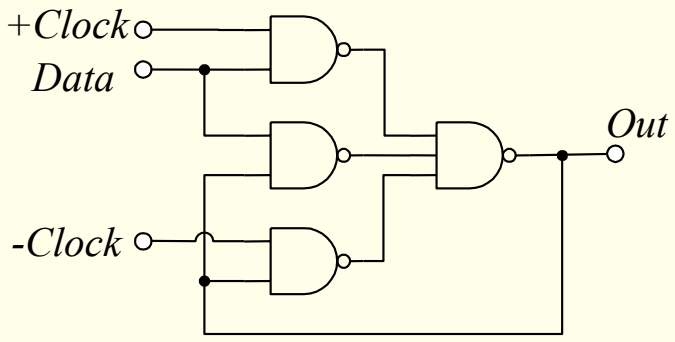
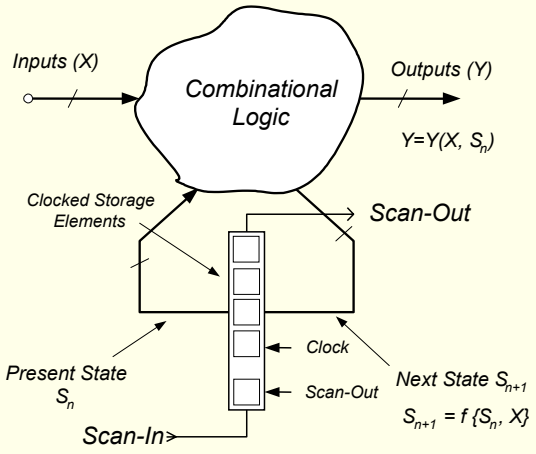
Hazard-Free Level-Sensitive Polarity-Hold Latch

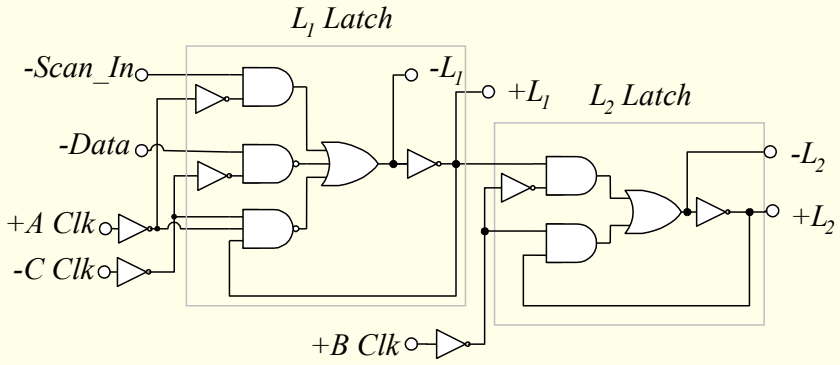


Eichelberger 1983

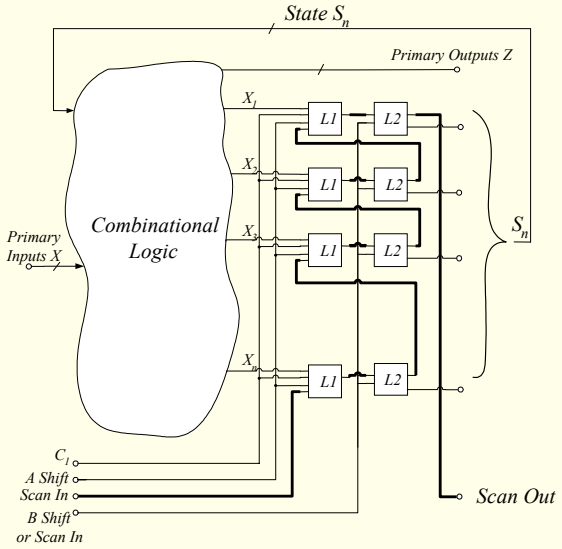
General LSSD Configuration



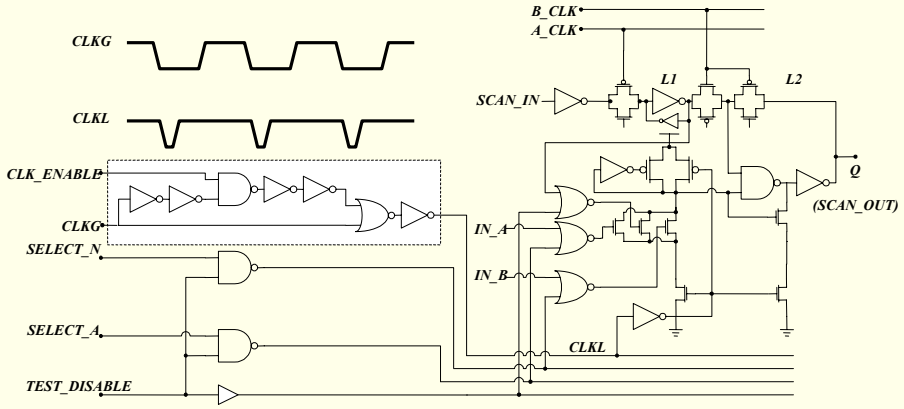
LSSD Shift Register Latch



LSSD Double Latch Design

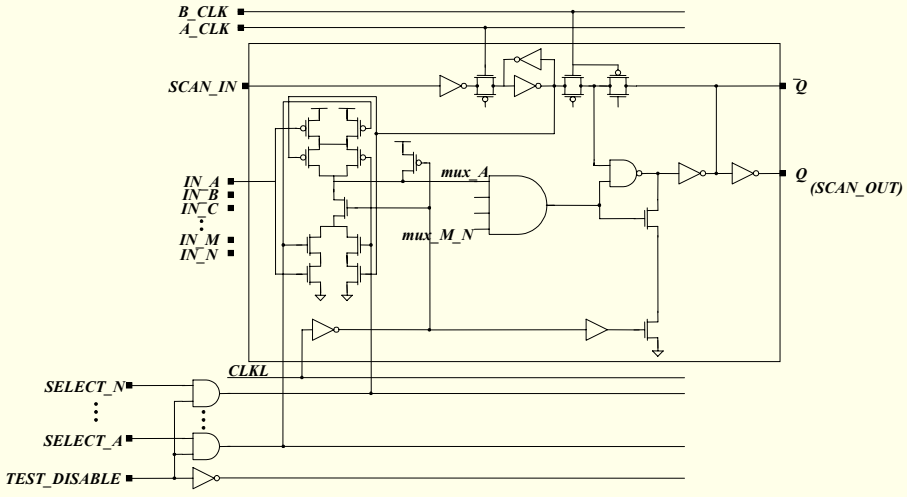


IBM® S/390 Parallel Server Processor



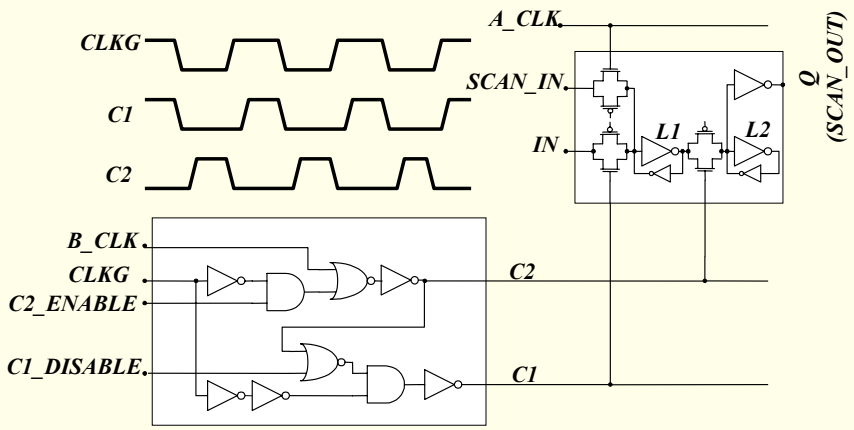
LSSD SRL with multiplexer used in the IBM S/390 G4 processor (Sigal et al. 1997), reproduced by permission

IBM® S/390 Parallel Server Processor



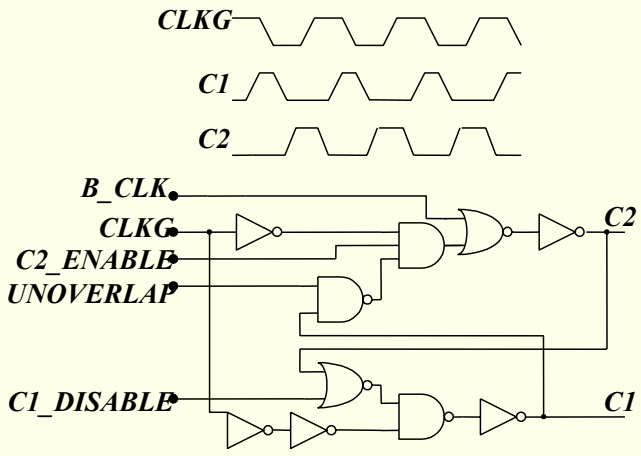
Static multiplexer version of the SRL used in the IBM S/390 G4 (Sigal et al. 1997), reproduced by permission

IBM® S/390 Parallel Server Processor



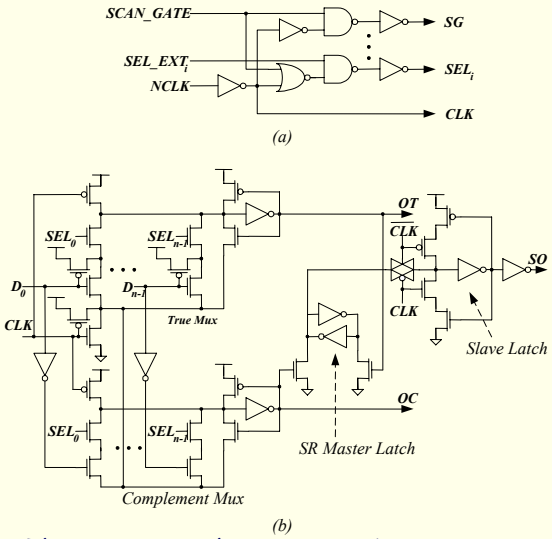
A clocked storage element is used in the non-timing-critical timing macros of the IBM S/390 G4 processor (Sigal et al. 1997), reproduced by permission

IBM® S/390 Parallel Server Processor



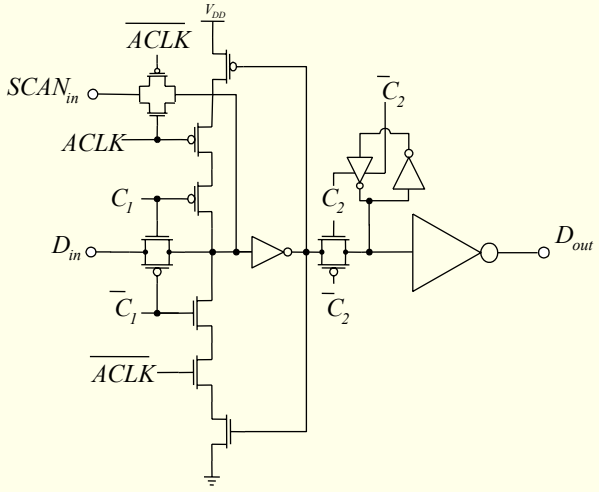
The clock-generation element used to detect problems created with fast paths: IBM S/390 G4 processor (Sigal et al. 1997), reproduced by permission

IBM® PowerPC Processor



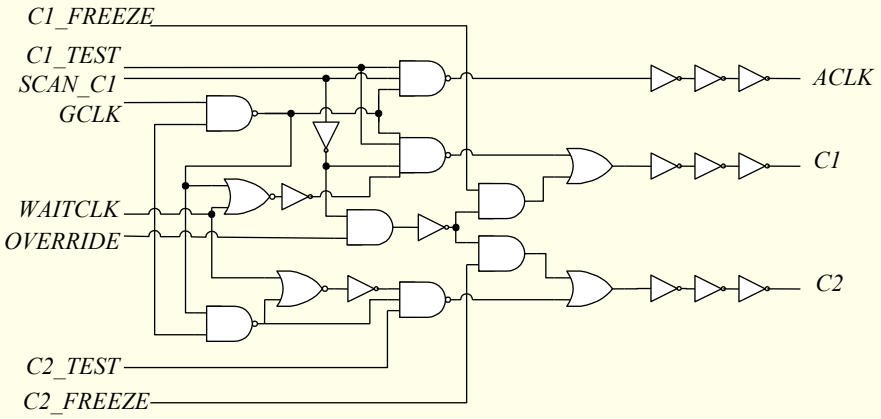
The experimental IBM PowerPC processor (Silberman et al. 1998), reproduced by permission

IBM® PowerPC 603: Master-Slave Latch



The PowerPC 603 MSL (Gerosa et al. 1994), Copyright © 1994 IEEE

IBM® PowerPC 603: Local Clk Generator



The PowerPC 603 local clock regenerator (Gerosa et al. 1994), Copyright © 1994 IEEE

Summary

- Intel® Microprocessors
  - Active clock deskewing in Pentium® processors
- Sun Microsystems® Processors
  - Semidynamic flip-flop (one of the fastest single-ended flip-flops today, "soft-edge")
- Alpha® Processors
  - Performance leader in the '90s
  - Incorporating logic into CSEs
- IBM® Processors
  - Design for testability techniques
  - Low-power champion PowerPC 603