Digital System Clocking:

High-Performance and Low-Power Aspects

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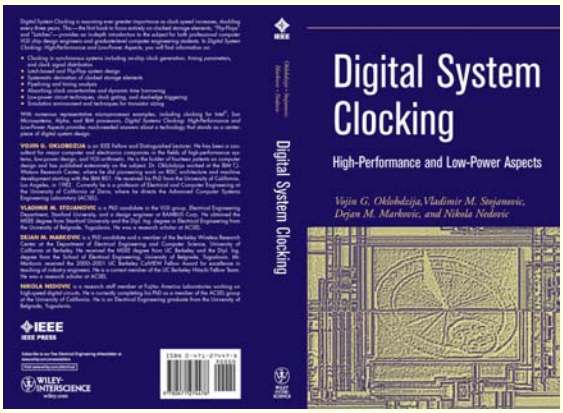
Chapter 8: State-of-the-Art Clocked Storage Elements in CMOS Technology

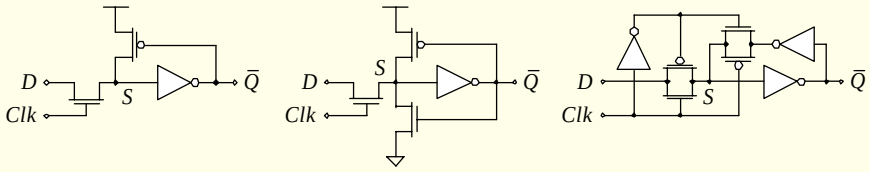


Wiley-Interscience and IEEE Press, January 2003

- Master-Slave Latches
- Flip-Flops
- CSE's with local clock gating
- Low clock swing
- Dual-edge triggering

Transmission gate latches

Simplest implementation *Basic static latch* *Complete implementation*



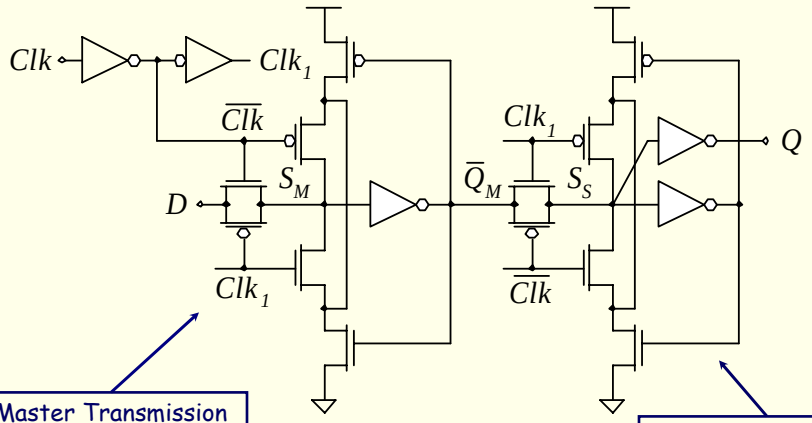
(a) (b) (c)

- *only 4 transistors*
- *Dynamic when S=1*
- *Susceptible to noise*

- *pull-up/pull-down keeper*
- *Conflict at node S whenever new data is written*

- *Feedback turned off when writing to the latch*
- *No conflict*
- *Larger clock load*

Transmission Gate Master-Slave Latch (MSL)

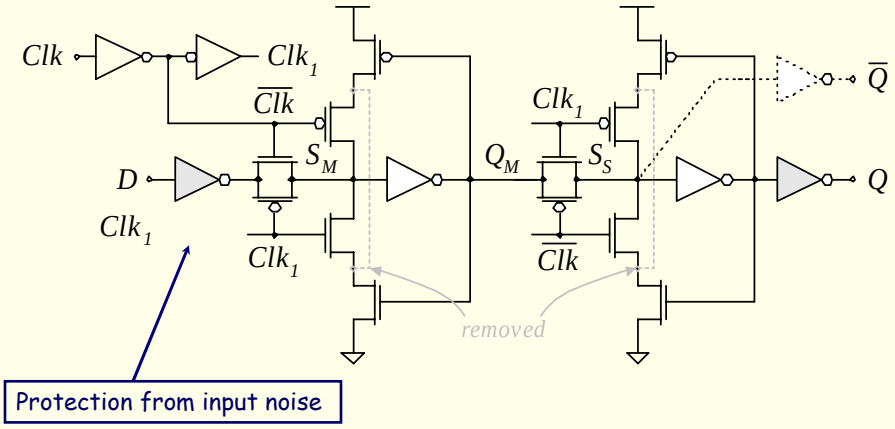


Master Transmission Gate Latch

Slave Transmission Gate Latch

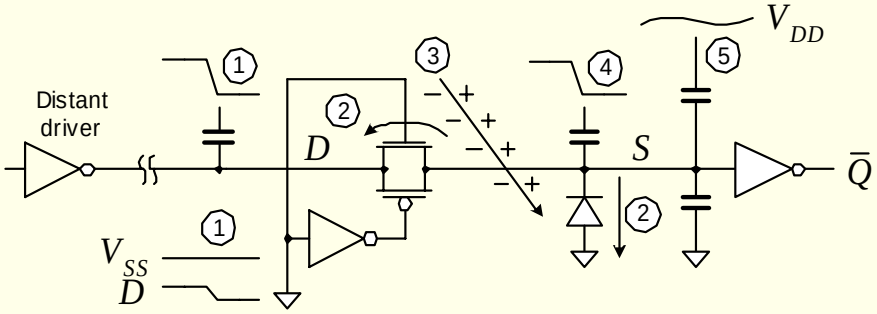
MSL with unprotected input
(Gerosa et al. 1994), Copyright © 1994 IEEE

Transmission Gate MS Latch (continued)



MSL with input gate isolation
(Markovic et al. 2001), Copyright © 2001 IEEE

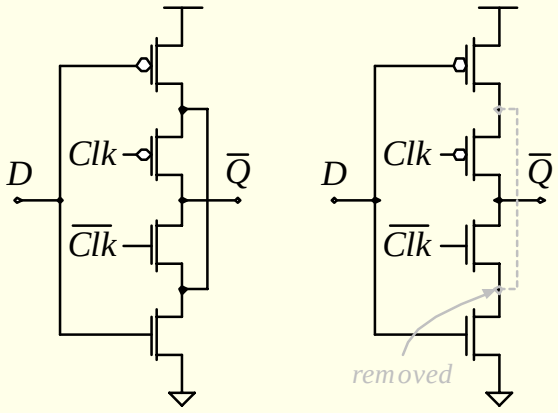
Noise Robustness of MS Latch



1. noise on input
2. leakage
3. α-particle and cosmic rays
4. unrelated signal coupling
5. power supply ripple

Sources of noise affecting the latch state node
(Partovi in Chandrakasan et al. 2001), Copyright © 2001 IEEE

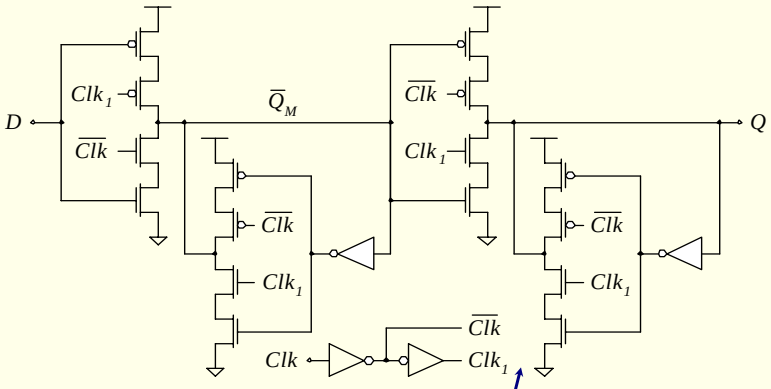
Clocked CMOS (C^2MOS) Latch



Transmission gate latch with gate isolation (dynamic)

C^2MOS latch (dynamic)

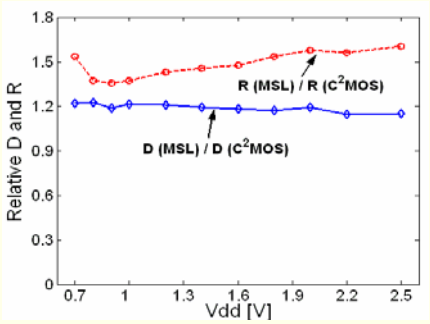
Clocked CMOS (C^2MOS) MS Latch



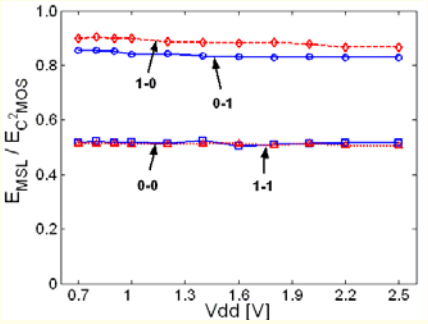
State-keeping feedbacks outside the D-to-Q path

(Suzuki et al. 1973), Copyright © 1973 IEEE

MS Latches: Comparison



Delay (D) and Race immunity (R)

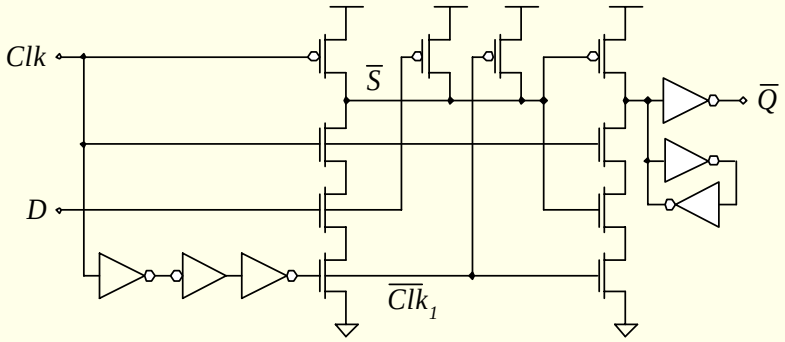


Energy per cycle

C^2MOS: larger clock transistors:
-Smaller delay and race immunity (80% of MSL)
-Higher energy consumption (1.4x more than MSL)

- Master-Slave Latches
- **Flip-Flops**
- CSE's with local clock gating
- Low clock swing
- Dual-edge triggering

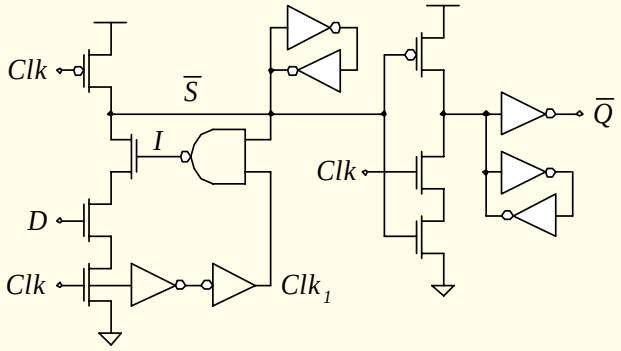
Hybrid Latch Flip-Flop (HLFF)



- Transparent to D only when Clk and $\overline{Clk_1}$ are both high
- Limited clock uncertainty absorption
- Small D→Q delay
- Small clock load

(Partovi et al. 1996), Copyright © 1996 IEEE

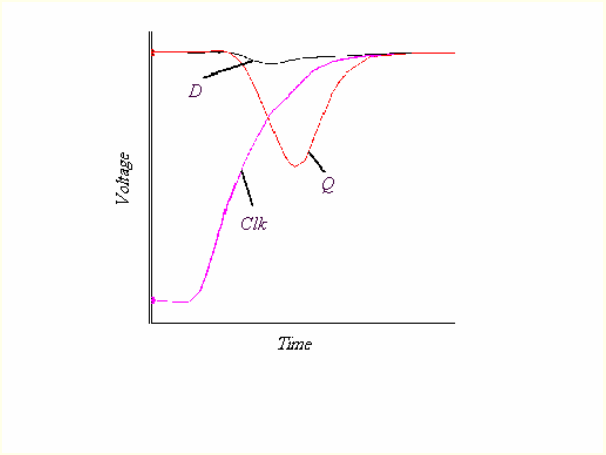
Semidynamic Flip-Flop (SDFF)



- Dynamic-style first stage
  - Fast, small clock load, logic embedding
  - Consumes energy for evaluation whenever D=1
- Dynamic-to-static latch in second stage
  - "Static 1" hazard

(Klass 1998), Copyright © 1998 IEEE

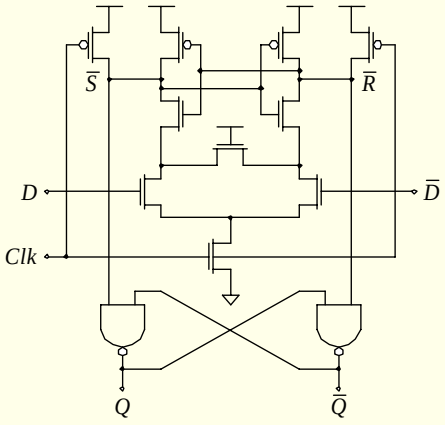
"Static 1" hazard in SDFF



- If D=Q=1 in previous cycle, race between Clk and $\overline{S}$ causes Q to falsely switch to 0 → generated glitch
- Also seen in HLFF

Sense-Amplifier Flip-Flop (SAFF)

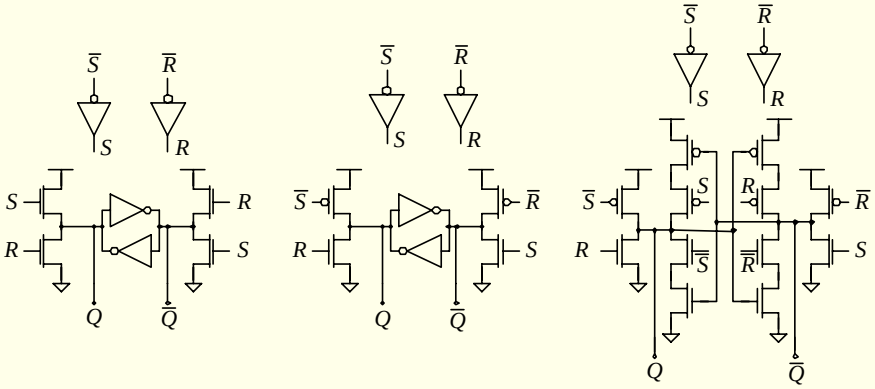
- When Clk=0, $\overline{S}$ and $\overline{R}$ are high, Q and $\overline{Q}$ unchanged
- At rising edge of Clk
  - sense amplifier in 1st stage generates a "low" pulse on either $\overline{S}$ or $\overline{R}$, based on which of D and $\overline{D}$ is higher
  - Other node $\overline{R}$ or $\overline{S}$ is driven high, preventing further changes
  - Latch captures low level of $\overline{S}$ or R and updates output



Both NAND gates must sequentially switch to change Q and Q

Original design (Montanaro et al. 1996), Copyright © 1996 IEEE

SAFF: Evolution of 2nd Stage Latch



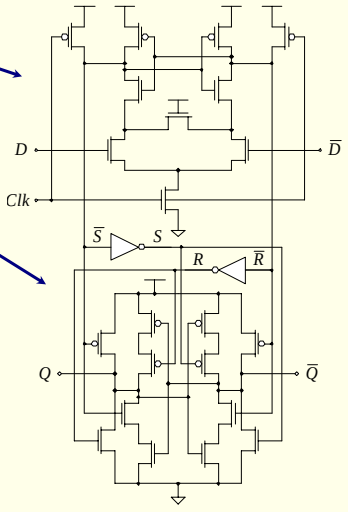
all-n-MOS push-pull (Gieseke et al. 1991);

complementary push-pull (Oklobdzija and Stojanovic 2001)

complementary push-pull with gated keeper (Nikolic, Stojanovic, Oklobdzija, Jia, Chiu, Leung 1999).

Modified Sense Amplifier Flip-Flop (MSAFF)

- Sense amplifier in 1st stage generates a "low" pulse on either $\overline{S}$ or $\overline{R}$, based on which of D and $\overline{D}$ is higher
- Symmetric latch in 2nd stage
  - outputs are simultaneously pulled to Vdd and Gnd → fast
  - Large drive capability → can be small
- Keeper in latch active only when there is no change
  - No conflict



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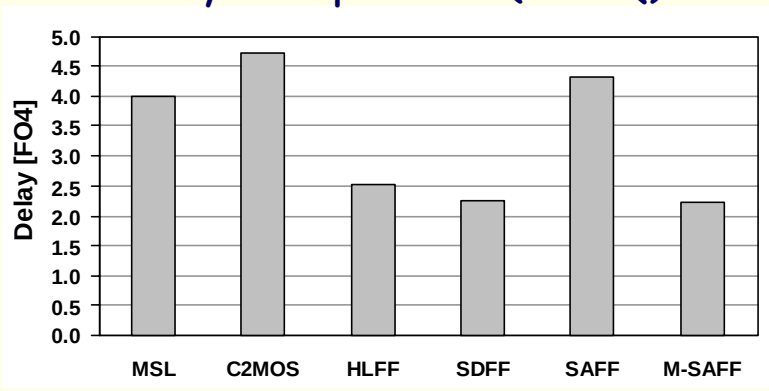
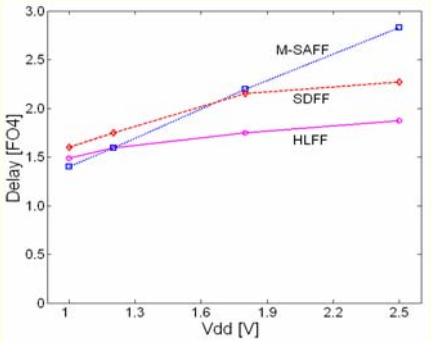
Flip-Flops and MS Latches: Delay Comparison (D→Q)

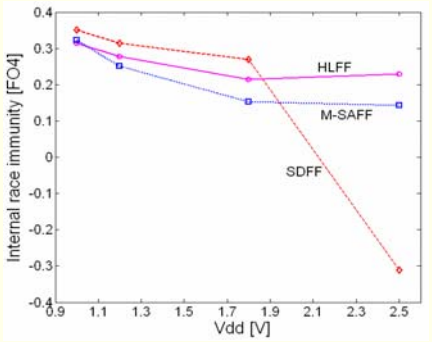


- MS Latches are slow – positive setup time, two latches in critical path
- SAFF is slow: it waits for one output to switch the other
- Fastest structures are simple flip-flops with negative setup time

CSE delay comparison (0.18 μm, high load)

Flip-Flops: Timing Comparisons with Voltage Scaling



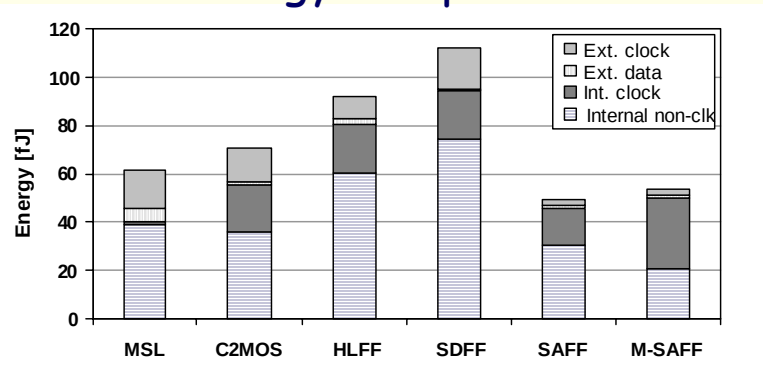


Delay comparison:
- *Relative delay reduces with supply voltage due to reduction of body effect*

Internal race immunity comparison:
- *Small race immunity, usually not a concern in critical paths*

(0.25 μm, light load)

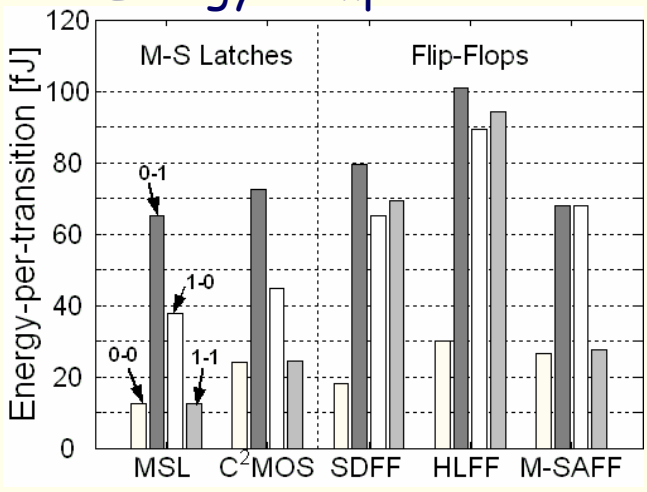
Flip-Flops and MS Latches: Energy Comparison



- In MS Latches, internal nodes change only when input D changes
- SAFF, M-SAFF: very small clock load, small 2nd stage latch
- Most energy consumed in HLFF, SDFF with pulse generator and high internal switching activity

CSE energy breakdown (0.18 μm, 50% activity, high load)

Flip-Flops and MS Latches: Energy Comparisons

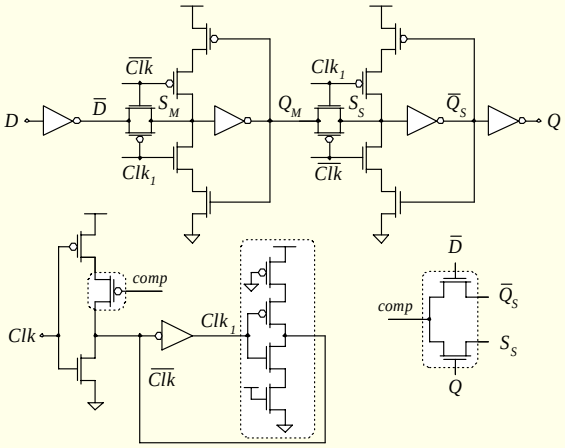


(0.25 μm, light load)
(Markovic et al. 2001), Copyright © 2001 IEEE

- Master-Slave Latches
- Flip-Flops
- CSE's with local clock gating
- Low clock swing
- Dual-edge triggering

Gated Transmission Gate MS Latch

- Concept: inhibit clock switching when new D = Q
  - *comp*=D XNOR Q
  - If *comp*=0 (D≠Q), circuit works as MSL
  - If *comp*=1 (D=Q), Clk=0, Clk_1=1 ⇒ latches closed, no output change, no internal power



Gated MSL
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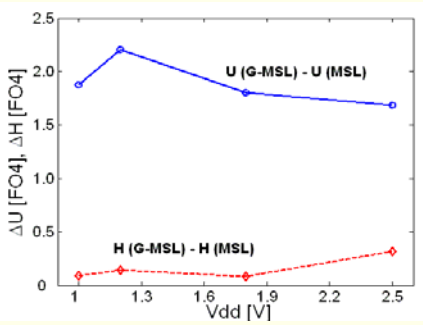
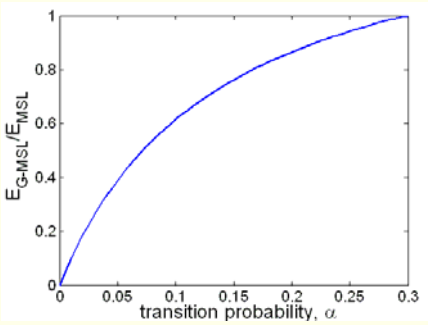
Gated TG MS Latch: Timing and Energy



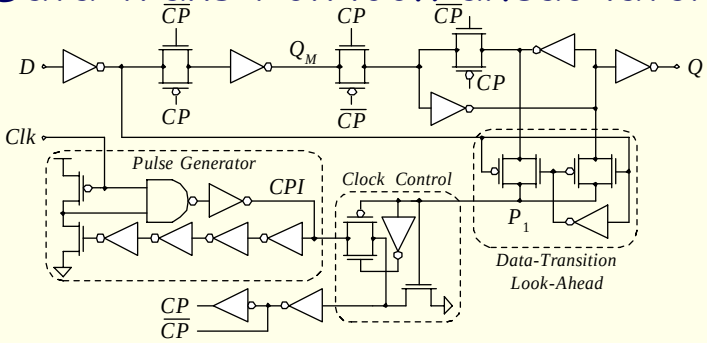
Setup time (U) and Hold time (H) comparison with MSL



Energy comparison with MSL

- Increased Setup time in gated MSL due to inclusion of the comparator into the critical path ⇒ slower than conventional MSL
- Smaller energy per transition if switching activity of D is <0.3
  - For higher switching activity, comparator and clock generator dominate the energy consumption

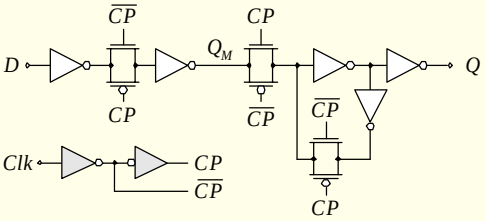
Data-transition look-ahead latch



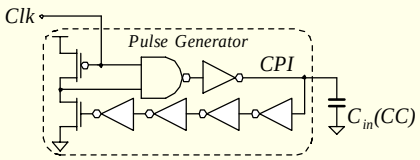
- Pulsed latch in which the generation of clock pulses are gated with XOR DTLA circuit
  - If D≠Q⇒ P_1=0, circuit operates as a conventional pulsed latch
  - If D=Q ⇒ P_1=1 ⇒ CP=0, no output change or energy consumption in the latch
- XOR circuit and Clock Control in the critical path → large setup time and D-Q delay

(Nogawa and Ohtomo 1998), Copyright © 1998 IEEE

DTLA-L: Analysis of Energy Consumption



DTLA-L without clock gating



DTLA-L Pulse Generator

$$E_{CMSL} = \frac{\alpha}{2}\cdot(E_{0-1}+E_{1-0}) + \frac{1-\alpha}{2}\cdot E_{Clk} + E_{Cin}$$

$$E_{DL-DFF} = \frac{\alpha}{2}\cdot(E_{0-1}+E_{1-0}) + \frac{1-\alpha}{2}\cdot E_{D-idle}$$

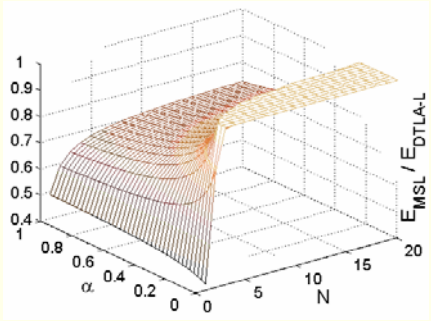
$$E_{0-1} = E_{D-idle} + E_{CLK} + E_{DL+CC} + E_{\text{int}} + E_{ext} \qquad E_{1-0} = E_{D-idle} + E_{CLK} + E_G + E_{\text{int}}$$

$$E_{D-idle} = E_{0-0} = E_{1-1} = \frac{E_{PG}}{N} + E_{Cin}$$

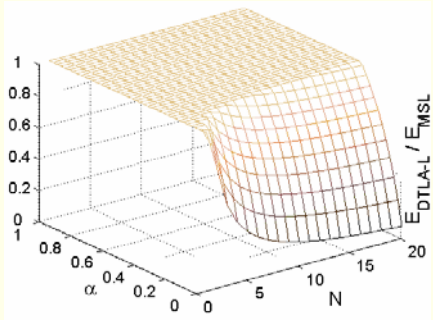
α – input switching activity

Pulse generator shared among N DTLA-L's

Energy comparison of DTLA-L and CMSL



E(DTLA-L) < E(CMSL)

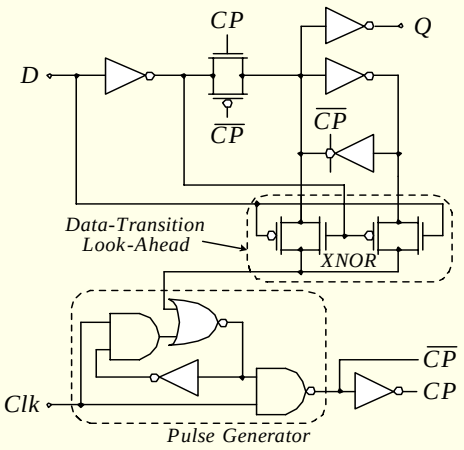


E(DTLA-L) > E(CMSL)

DTLA-L is more energy-efficient than CMSL when N>2 and α< 0.25

Clock-on-demand PL

- Pulsed latch in which the generation of clock pulses are gated with XNOR DTLA circuit
  - If D≠Q⇒ XNOR=0, CP→1 when Clk↑, and CP→0 after Q has changed to D
  - If D=Q ⇒ XNOR=1 ⇒ CP=0, no output change or energy consumption in the latch
- Pulse Generator includes clock control
  - can not be shared among multiple PL's



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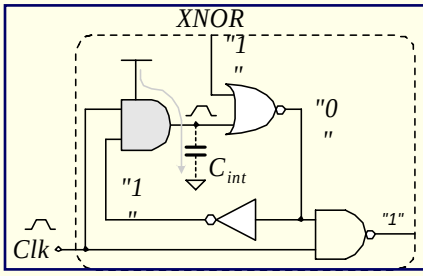
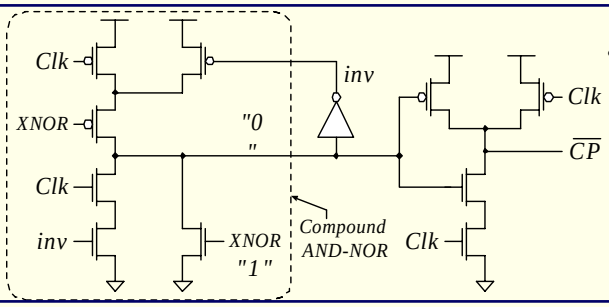
Energy-Efficient Pulse Generator in COD-PL

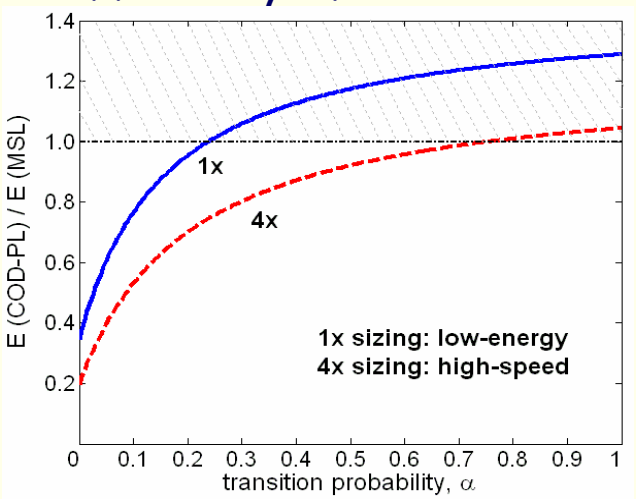


- Straightforward implementation with CMOS gates
  - C_{int} switches in each cycle
  - Energy-inefficient



- Compound AND-NOR gate
  - Energy-efficient

Impact of circuit sizing on the energy efficiency of COD-PL



COD-PL more effective in high-speed sizing due to large clock transistors

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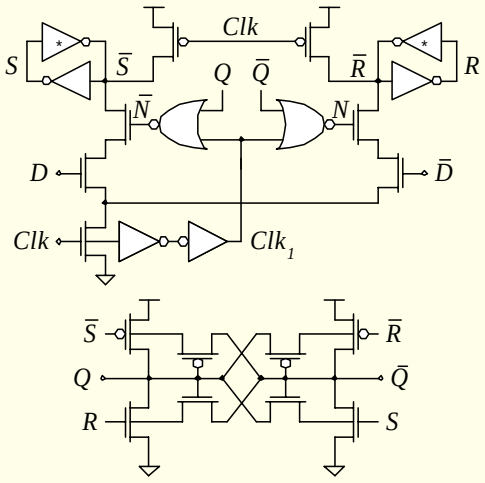
Conditional capture flip-flop

- First stage: pulse generator with internal clock gating
  - When Clk=1, $\overline{S}$=$\overline{R}$=1
  - When Clk=1, Clk_1=0, $\overline{S}$ can switch low if D=1, Q=0, $\overline{R}$ can switch low if D=0, Q=1
  - Otherwise, $\overline{S}$=$\overline{R}$=1 → no energy consumption
- Second stage: pass-gate implementation of M-SAFF latch (Oklobdzija, Stojanovic)
- *No setup time degradation due to clock gating*



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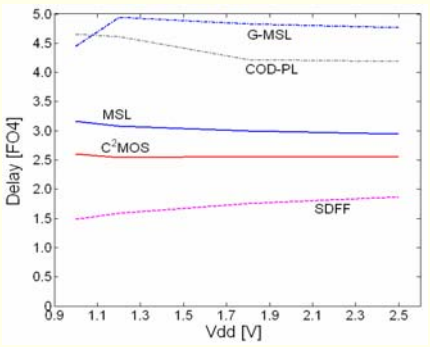
Comparison of latches and flip-flops with local clock gating: Timing



Delay comparison:
- *Delay relatively constant with supply voltage*
- *Latches with clock gating have very large delay due to large setup time*

Internal race immunity comparison:
- *Generally R(FF)< R(MSL)< R(gated MSL)*
- *COD-PL has low race immunity due to wide clock pulse*

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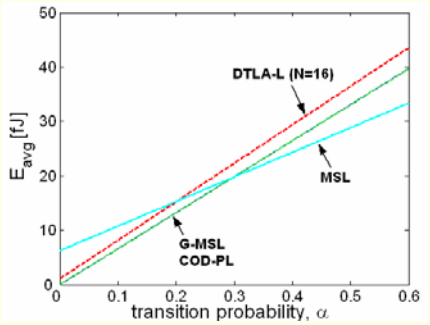
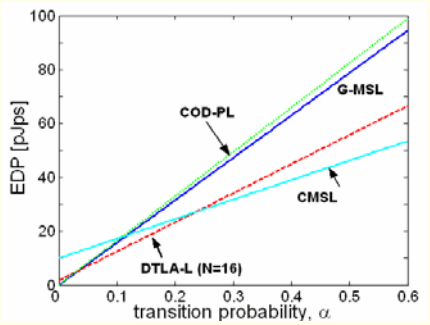
Comparison of latches and flip-flops with local clock gating: Energy, EDP





Energy comparison:
- *Latches with gated clock consume less energy than MSL if α < 0.2 – 0.3*

Energy-Delay Product comparison:
- *α < 0.03 ⇒ G-MSL best*
- *0.03 < α < 0.23 ⇒ DTLA-L best*
- *0.23 < α ⇒ Conventional MSL best*

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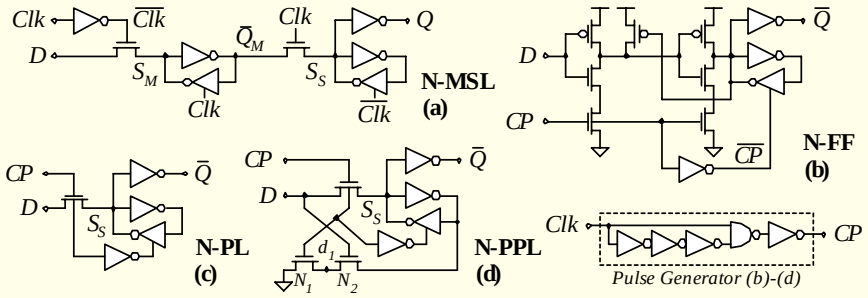
- Master-Slave Latches
- Flip-Flops
- CSE's with local clock gating
- Low clock swing
- Dual-edge triggering

N-only clocked latches

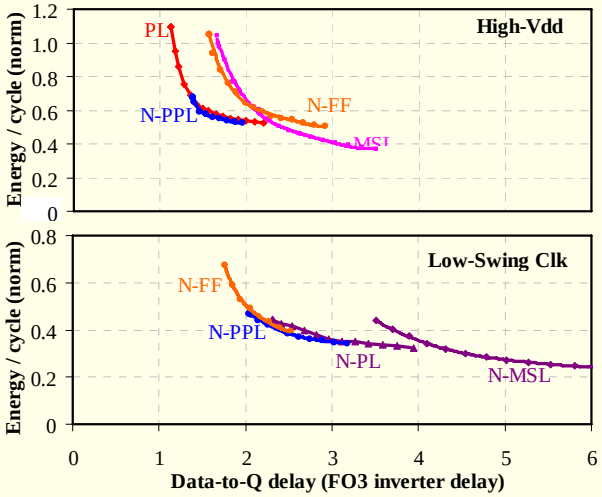


- Concept: Bring clock only to n-MOS transistors to allow reduced clock swing without conflict with partially turned-off p-MOS transistors
- Reduced clock swing reduces clocking energy with some penalty in performance
  - Clock is always in critical path as its edge signalizes when to change the output

(a) conventional TG MSL, (b) pulsed-latch, (c) conventional PL, (d) push-pull PL

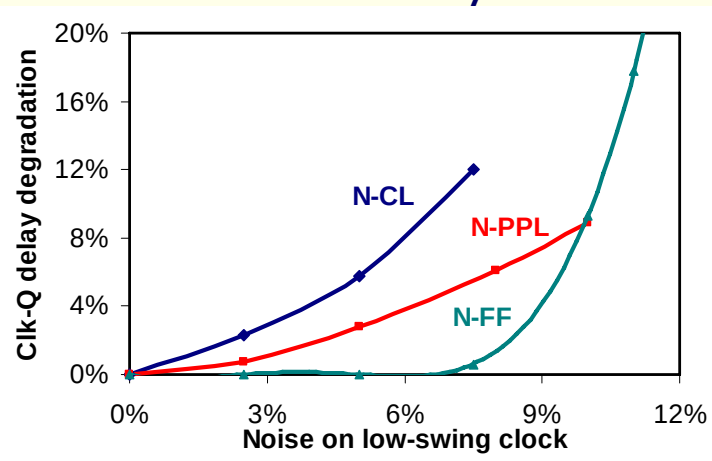
Low clock swing CSE's comparison: energy and delay

- Full-swing:
  - PL preferred for high-speed
  - MSL preferred for low energy
- Low-swing clock:
  - N-FF preferred for high-speed
  - N-PPL is preferred for low energy



130nm technology, 50fF load, max. input cap=12.5fF, data activity=0.1: (a) high-V_{dd} and (b) low-swing Clk

Effect of clock noise on low-swing clock latch delay

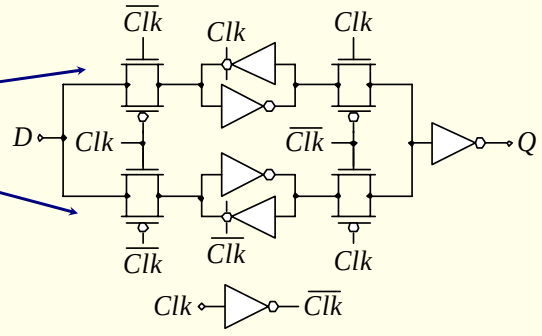


- All latches fail for clock noise > 12% of clock voltage
- N-FF gives best clock noise rejection

- Master-Slave Latches
- Flip-Flops
- CSE's with local clock gating
- Low clock swing
- Dual-edge triggering

DET Latch-mux circuit (DET-LM)

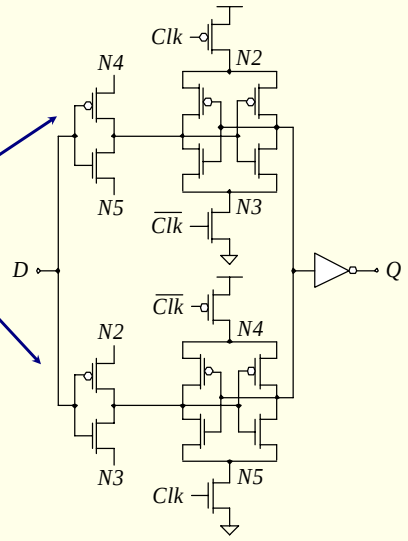
- Pass-gate latches:
  - One transparent when Clk=0
  - One transparent when Clk=1
- Pass-gate multiplexer that selects the output of the opaque latch



(Llopis and Sachdev 1996), Copyright © 1996 IEEE

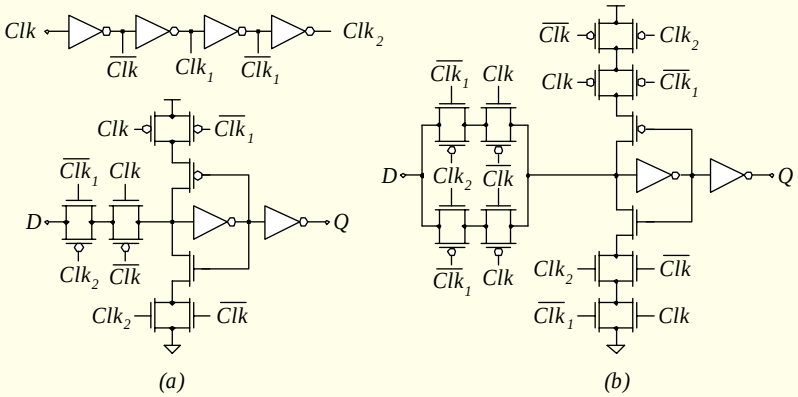
C²MOS Latch-mux (C²MOS-LM)

- C²MOS latches:
  - One transparent when Clk=1
  - One transparent when Clk=0
- Multiplexer: two C²MOS inverters that propagate the output of the opaque latch
- Large clock transistors shared between the latches and the multiplexer



(Gago et al. 1993), Copyright © 1993 IEEE

Pulsed-latch (DET-PL)

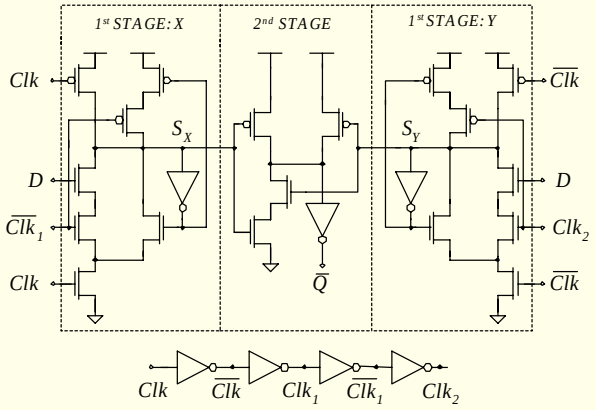


- Pulse generator transparent to D only when Clk=$\overline{Clk_1}$=1, or when $\overline{Clk}$=Clk_2=1 ⇒ shortly after both edges of the clock
- DET PL consumes lot of energy for four clocked pass gates
- To improve speed, modified from original design (Strollo et al, 1999) which implemented n-MOS-only pass gate and p-MOS-only keeper

(a) single - edge, (b) dual - edge triggered

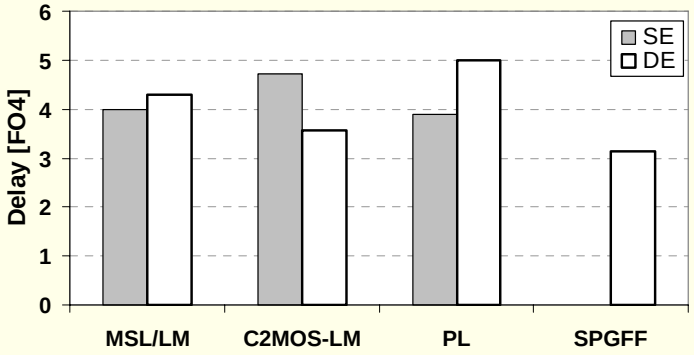
DET Symmetric pulse generator flip-flop (SPGFF)

- Two pulse generators: X active at rising edge of the clock, Y active at falling edge of the clock
- S_X and S_Y alternately precharge and evaluate
  - At any moment, one of S_X and S_Y keeps the value of data sampled at the most recent clock edge
  - The other S_X or S_Y is precharged high



- *Pulses at S_X and S_Y have same width as clock*
- *Second stage is a simple NAND gate ⇒ no need for a latch*

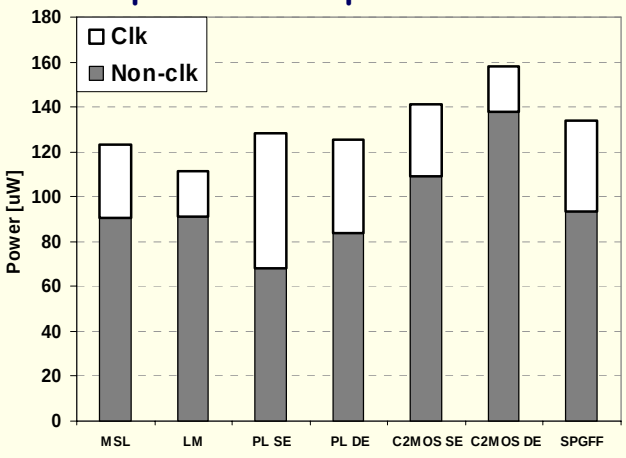
SET vs. DET: Delay comparison



- Latch-MUX's have two equally critical paths, somewhat shorter than that of MSL
- PL is more complex, adding more capacitance to the critical path compared to SET PL
- SPGFF has short domino-like critical path ⇒ fastest

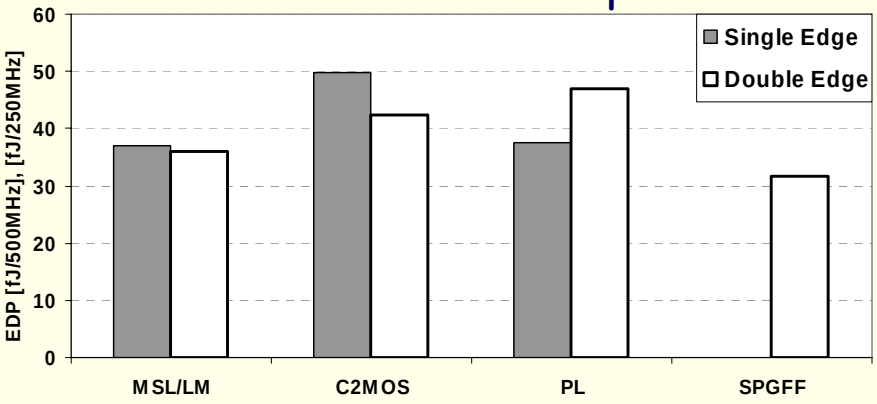
SET vs. DET: Power consumption comparison

- LM's benefit from clever implementation of latch-mux structure with clock transistors sharing
- PL adds extra high-activity capacitance compared to SET PL
- SPGFF power consumption is in the middle, mainly due to alternate switching of nodes S_X and S_Y



(0.18 μm, 500MHz for SET, 250MHZ for DET, high load)

SET vs. DET: EDP comparison



- Latch-MUX's have similar or better EDP than their SET counterparts
- PL exhibits worse delay and energy compared to SET PL, due to more complex design
- SPGFF is fastest with moderate energy consumption: lowest EDP
- EDP (SPGFF) < EDP (LM) < EDP (PL)

(0.18 μm, 500MHz for SET, 250MHZ for DET high load)