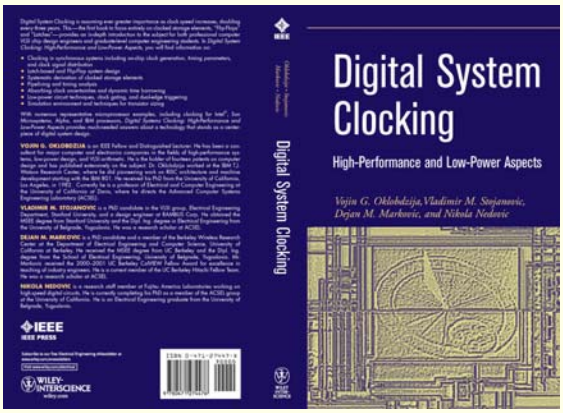
Digital System Clocking:

High-Performance and Low-Power Aspects

Vojin G. Oklobdzija, Vladimir M. Stojanovic, Dejan M. Markovic, Nikola M. Nedovic

Chapter 6: Low-Energy System Issues



Wiley-Interscience and IEEE Press, January 2003

Clocking Energy

- System Issues
  - Increasing clock frequency
  - Low skew requirements
  - Deeper pipelining
- Increased Clocking Energy
  - Focus on energy minimization
- Methods for Energy Reduction
  - Supply voltage scaling
  - Alternate circuit topology
  - New clocking strategies

Switching Energy

Clock is the highest activity signal ⇒ Switching energy is dominant

$$E_{switching} = \sum_{i=1}^{N} \alpha_{0-1}(i) \cdot C_i \cdot V_{swing}(i) \cdot V_{DD}$$

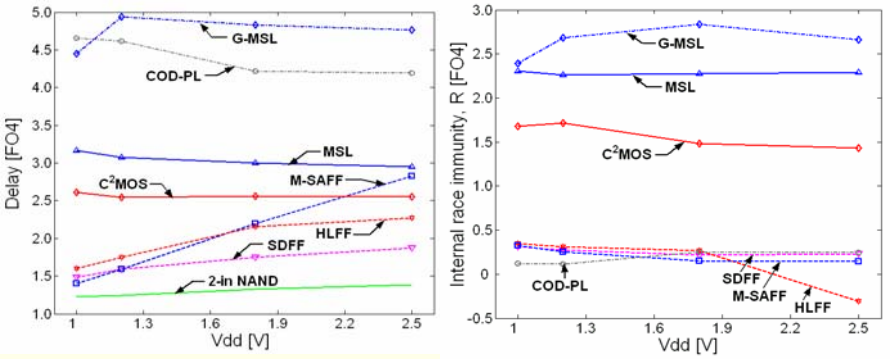
α - probability of a 0-1 transition
C_i – total switched capacitance at node i
$V_{swing}(i)$ – voltage swing at node i
V_{DD} – supply voltage
N – number of nodes

Energy is best reduced by scaling down V_{DD}, but this also means performance degradation

Supply Voltage Scaling

- Supply voltage is the most dominant tuning knob for energy reduction
  - Not always possible due to performance requirements
- Flip-flop speed scales favorably with Vdd compared to standard CMOS inverter
  - Improved slow-path requirements
- Internal race immunity tracks scaling of an inverter
  - Same fast-path requirements

Pulsed Designs Scale the Best with V_{DD}



(a) *(b)*

(Delay is normalized to FO4 at its respective V_{DD}. FO4 as defined in this example increases with V_{DD} ⇒ performance degradation)

Impact of Vdd on (a) delay, and (b) internal race immunity (0.25 μm, light load). (Markovic et al. 2001), Copyright © 2001 IEEE

Minimizing Switched Capacitance

- Clocked capacitances are the most important to minimize due to their high switching activity
- Reduce Csw by circuit sizing that takes into account both energy and performance
  - Topology dependent
  - Lower limit imposed by the noise requirements

Other Energy Reduction Techniques

- Low-Swing Circuit Techniques
  - Reduced-swing Clk drivers
  - CSE redesign
  - N-only CSEs with Low-Vcc Clk
- Clock Gating
  - Global
  - Local
- Dual-Edge Triggering
  - Latch-mux
  - Pulsed-latch
  - Flip-flop

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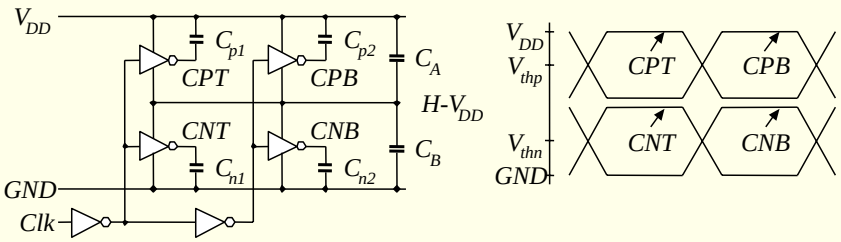
Low-Swing Clocking, Option #1: Clock Driver Re-design

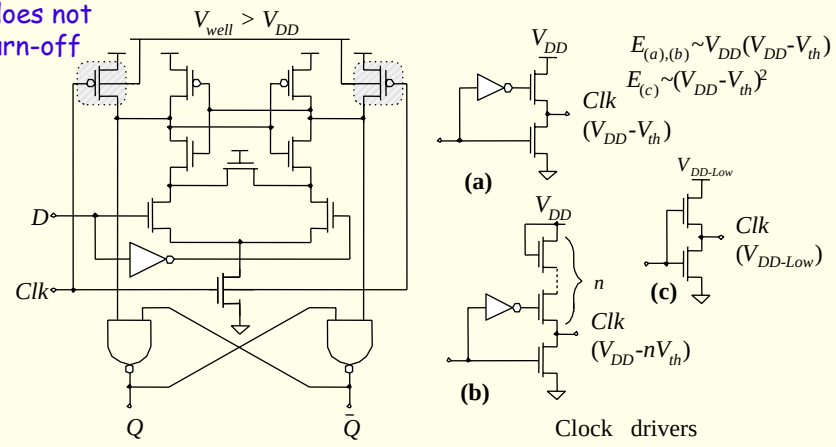


50% power reduction with half-swing clock
(minus some penalty in clock drivers)

Clock driver for half-swing clocking
(Kojima at al. 1995), Copyright © 1995 IEEE

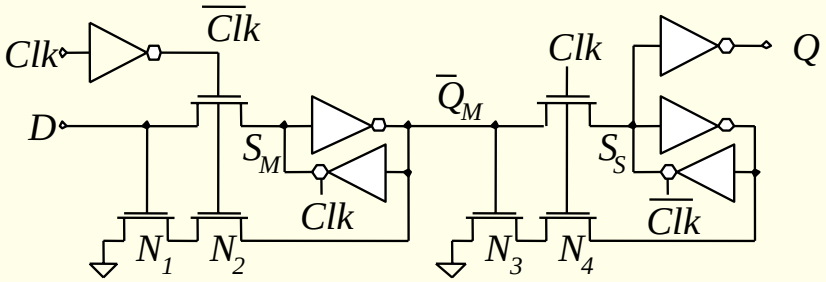
Low-Swing Clocking, Option #2: CSE Re-design

PMOS does not fully turn-off



Reduced clock-swing flip-flop
(Kawaguchi and Sakurai, 1998), Copyright © 1998 IEEE

Low-Swing Clocking, Option #3: N-only CSEs



N-only clocked transistors, M-S Latch Example
(N_1 and N_2 improve pull-up on S_M)

N-Only clocked M-S latch

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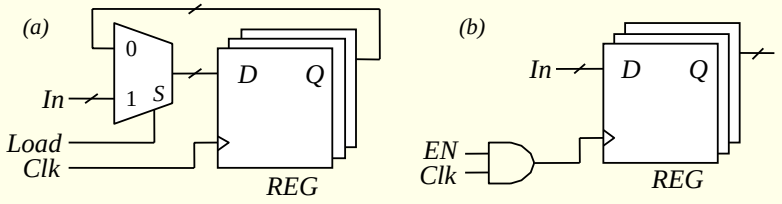
Clock Gating, Option #1: Global Clock Gating



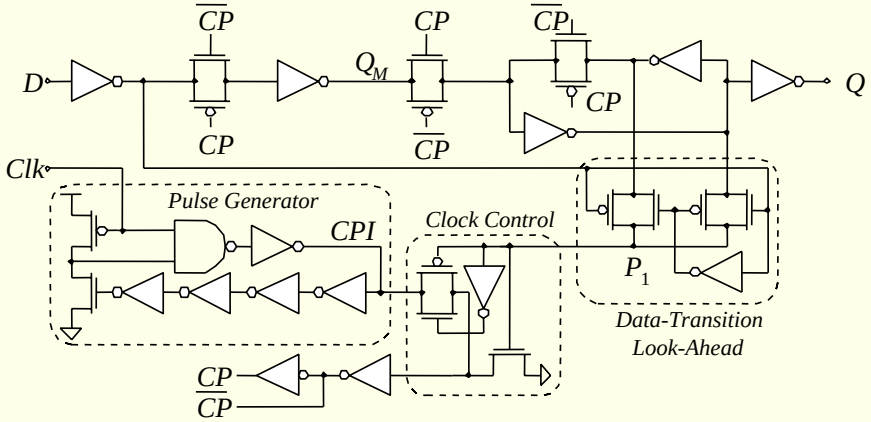
Time-mux (no gating!)

Global Clk Gating

Used to save clocking energy when data activity is low

(a) Nongated clock circuit, (b) gated clock circuit. (Kitahara et al. 1998), Copyright © 1998 IEEE

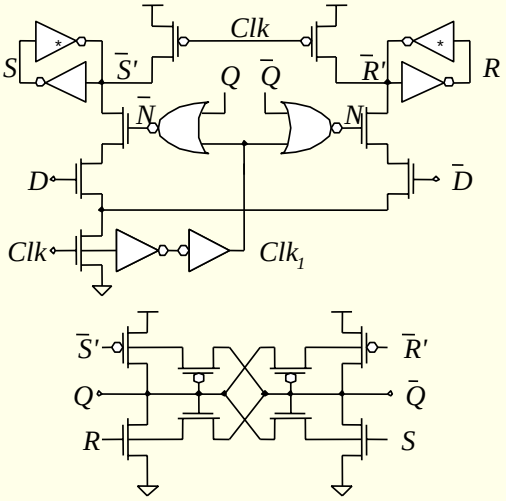
Clock Gating, Option #2: Local Clock Gating



Data-transition look-ahead latch (Nogawa and Ohtomo, 1998), Copyright © 1998 IEEE

Local Clock Gating, Another Example

Clk enabled only when D ≠ Q



Conditional capture flip-flop
(Kong et al. 2000), Copyright © 2000 IEEE

Other Energy Reduction Techniques

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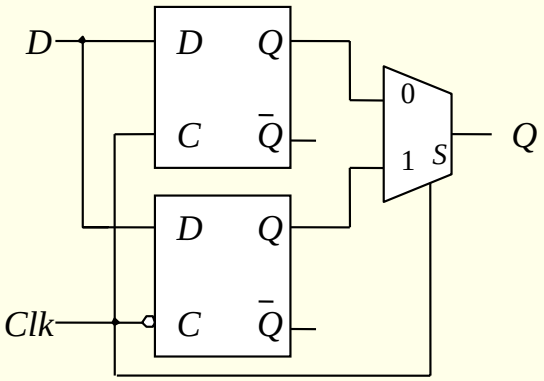
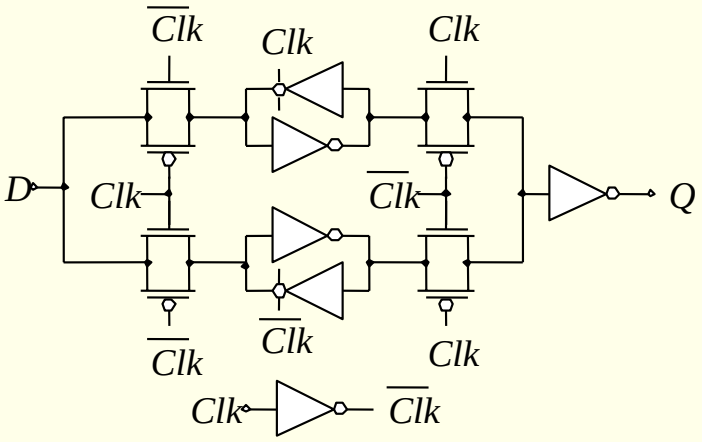
Dual-Edge Triggering, Option #1: Latch-Mux



Used to save clocking energy regardless of data activity!

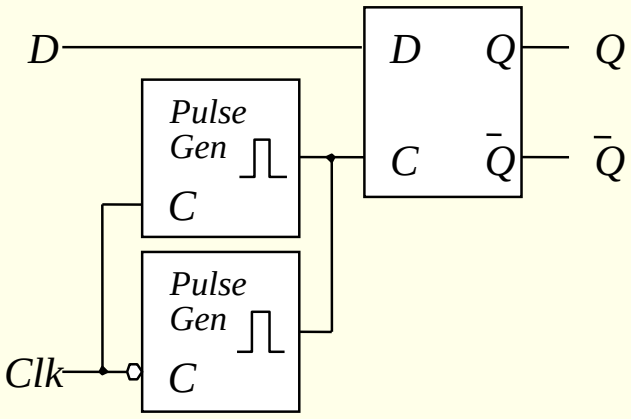
Dual-edge-triggered latch-mux design

DET Latch-Mux: Circuit Example



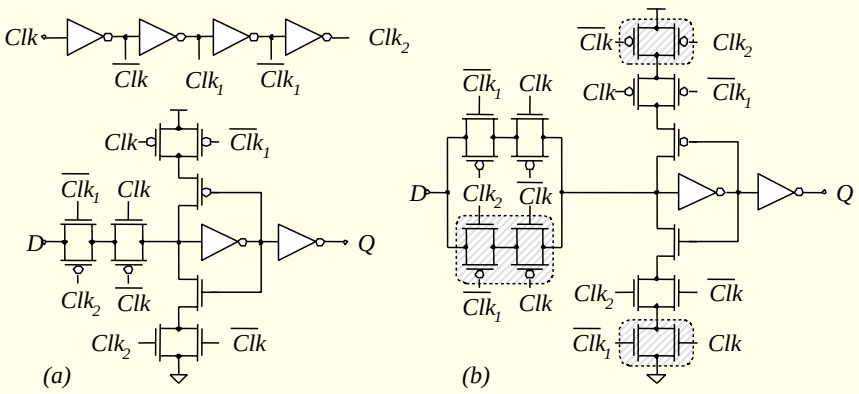
Dual-edge-triggered latch-mux circuit
(Llopis and Sachdev, 1996), Copyright © 1996 IEEE

Dual-Edge Triggering, Option #2: Pulsed-Latch



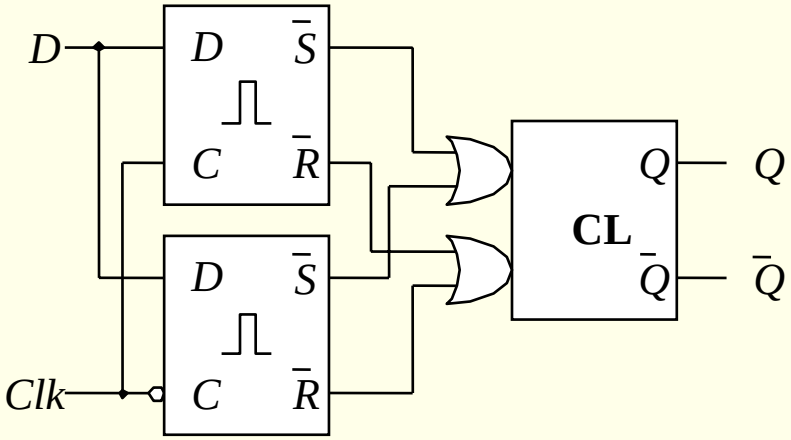
Dual-edge-triggered pulsed-latch design

DET Pulsed-Latch: Circuit Examples



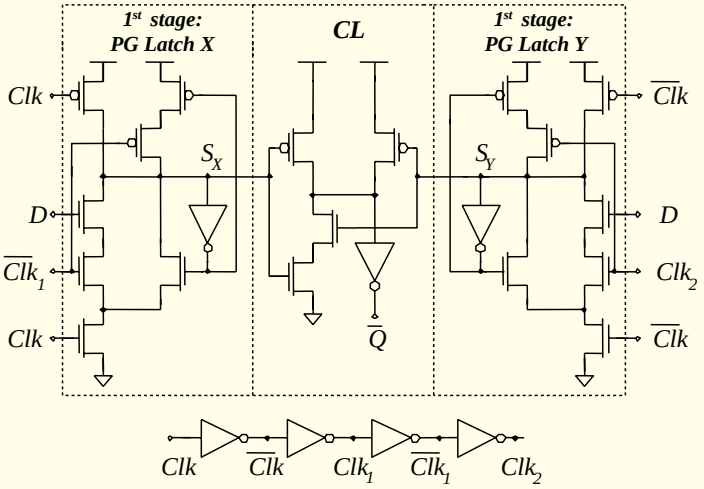
Pulsed-latch: (a) single-edge-triggered; (b) dual-edge-triggered

Dual-Edge Triggered Flip-Flop



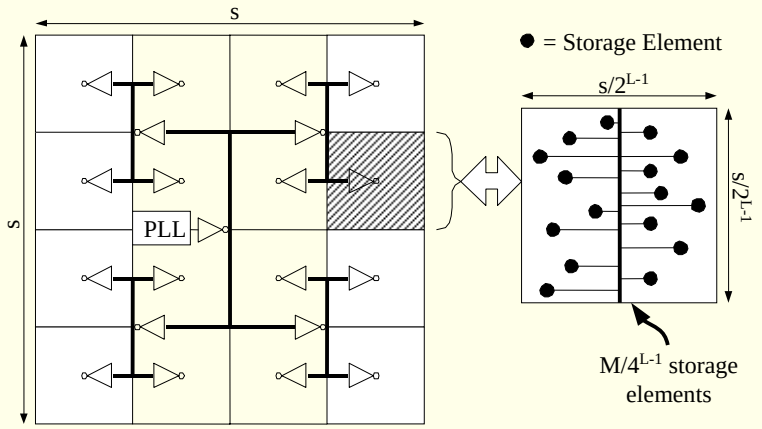
Dual-edge-triggered flip-flop design

DET Flip-Flop: Circuit Example



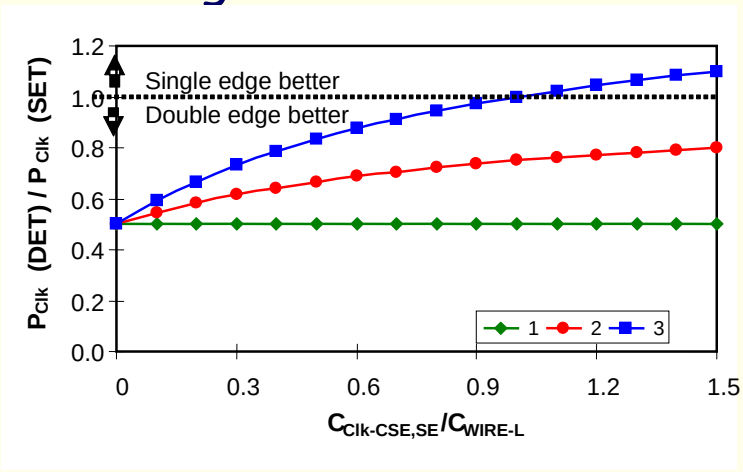
DET symmetric pulse-generator flip-flop

Clock Distribution for DET CSEs



H-tree clock distribution network

Clocking Power: SET vs. DET

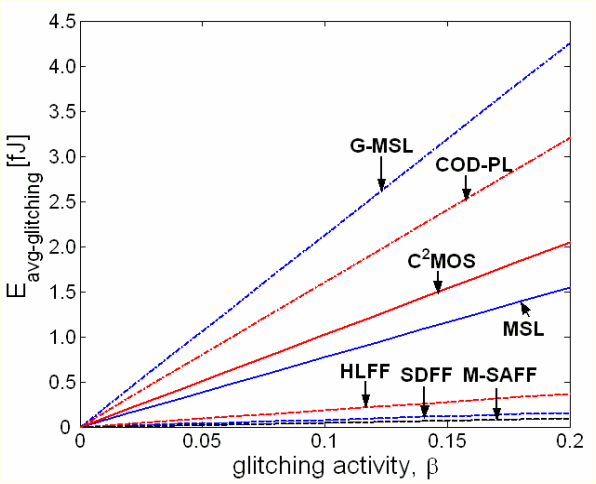


DET wins if the total clock load capacitance is below 2x the capacitance of a SET design

Glitch Tolerant Design

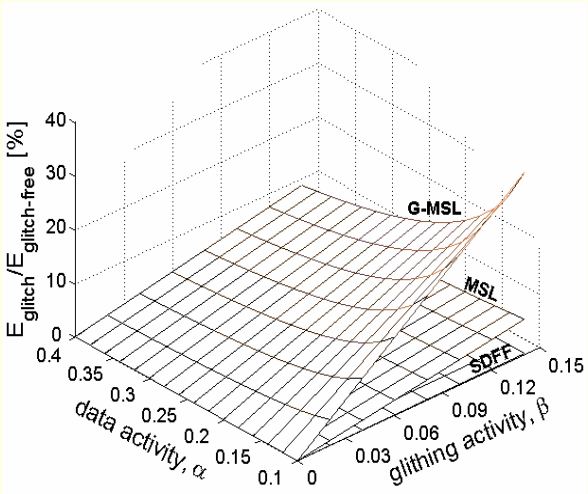
- Are CSEs that are the best in terms of active power also favorable in terms of glitch power?
- The opposite is true
- So, let's investigate how glitch power scales with data and glitching activity

Average Glitching Energy in CSEs



Comparison of average glitching energy in CSEs (Markovic at al. 2001), Copyright © 2001 IEEE

Comparison of $E_{glitching}$ and $E_{switching}$



Glitching energy as a percentage of switching energy in representative CSEs showing the greatest glitch sensitivity of the gated designs

Summary

- Energy best reduced by V_{DD} scaling
  - Penalty in performance
- Reducing Clk swing only reduces E_{Clk}
  - Still penalty in performance
- Clock gating
  - Reduces E_{Clk} at low-activity
  - No penalty in perf. if gating is outside crit-path
- Dual-Edge Triggering
  - Reduces E_{Clk} ideally by 2x
  - Small or no performance degradation