Digital System Clocking:

High-Performance and Low-Power Aspects

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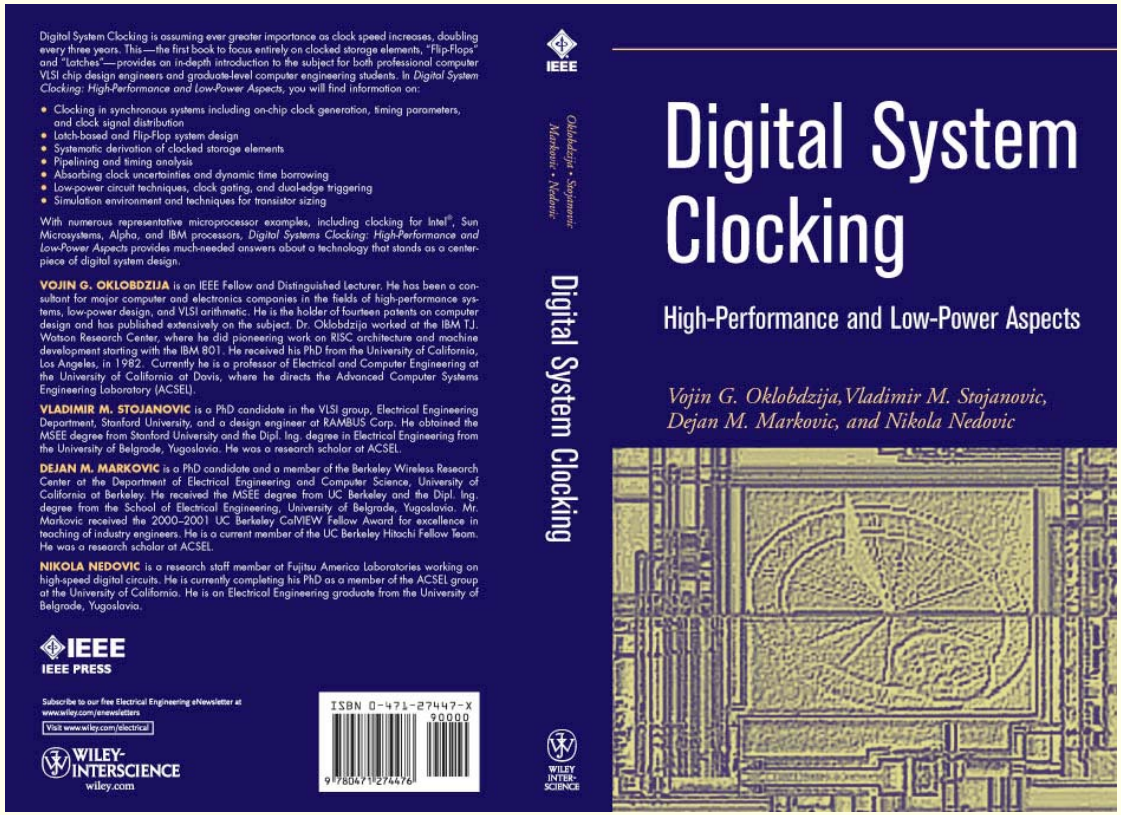
Chapter 5: High-Performance System Issues



Wiley-Interscience and IEEE Press, January 2003

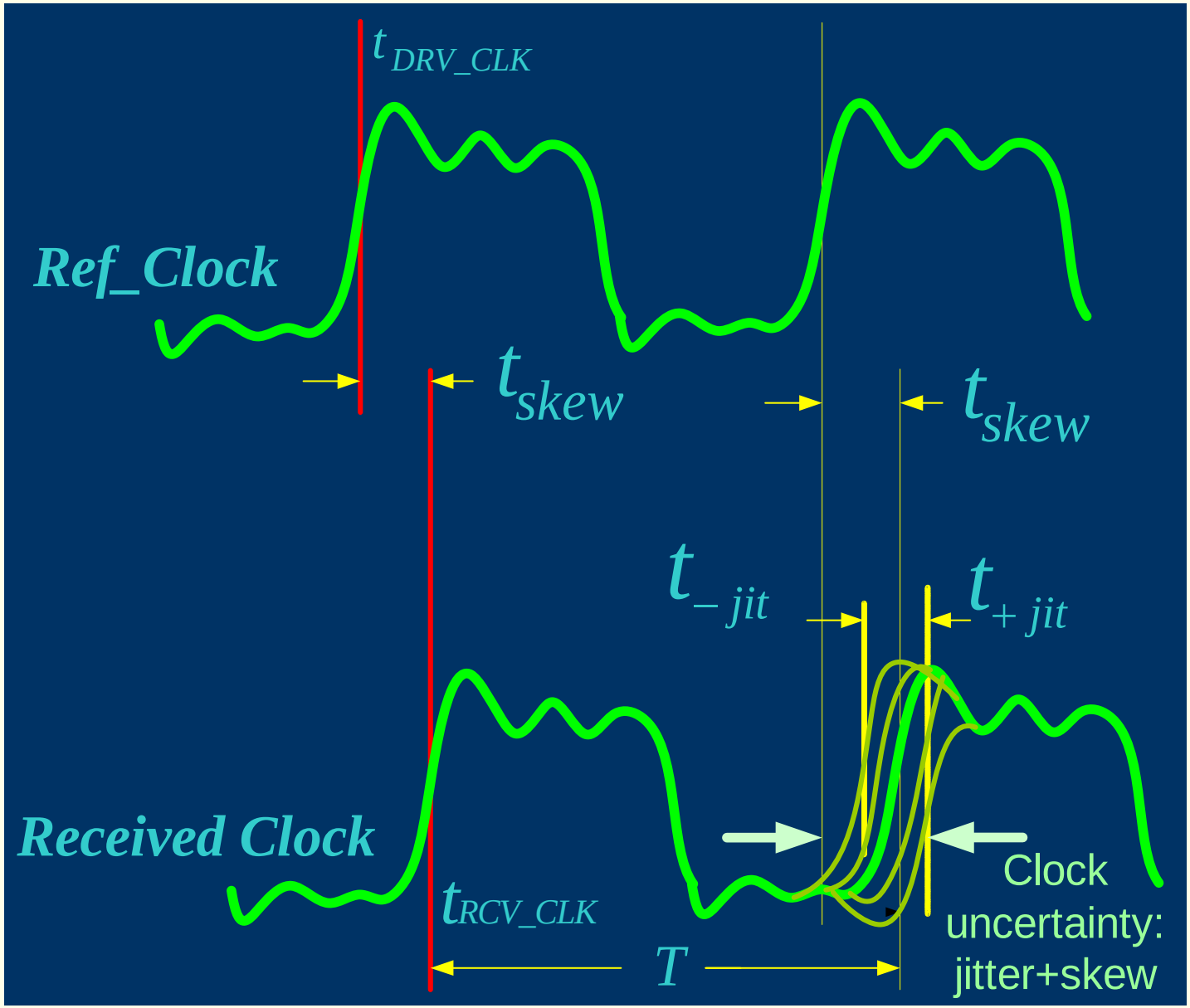
Absorbing Clock Uncertainties

- Clock uncertainties
  - Clock skew
  - Clock jitter
- Trends:
  - Clock distribution becomes progressively difficult due to:
    - load mismatch
    - Process, voltage, and temperature variations.
  - The clock uncertainties occupy increasing portion of the cycle time; typically 2 FO4.
- The ability to reduce impact of these uncertainties is one of the most important properties of the high-performance system.

Clock Generation and Distribution Non-idealities

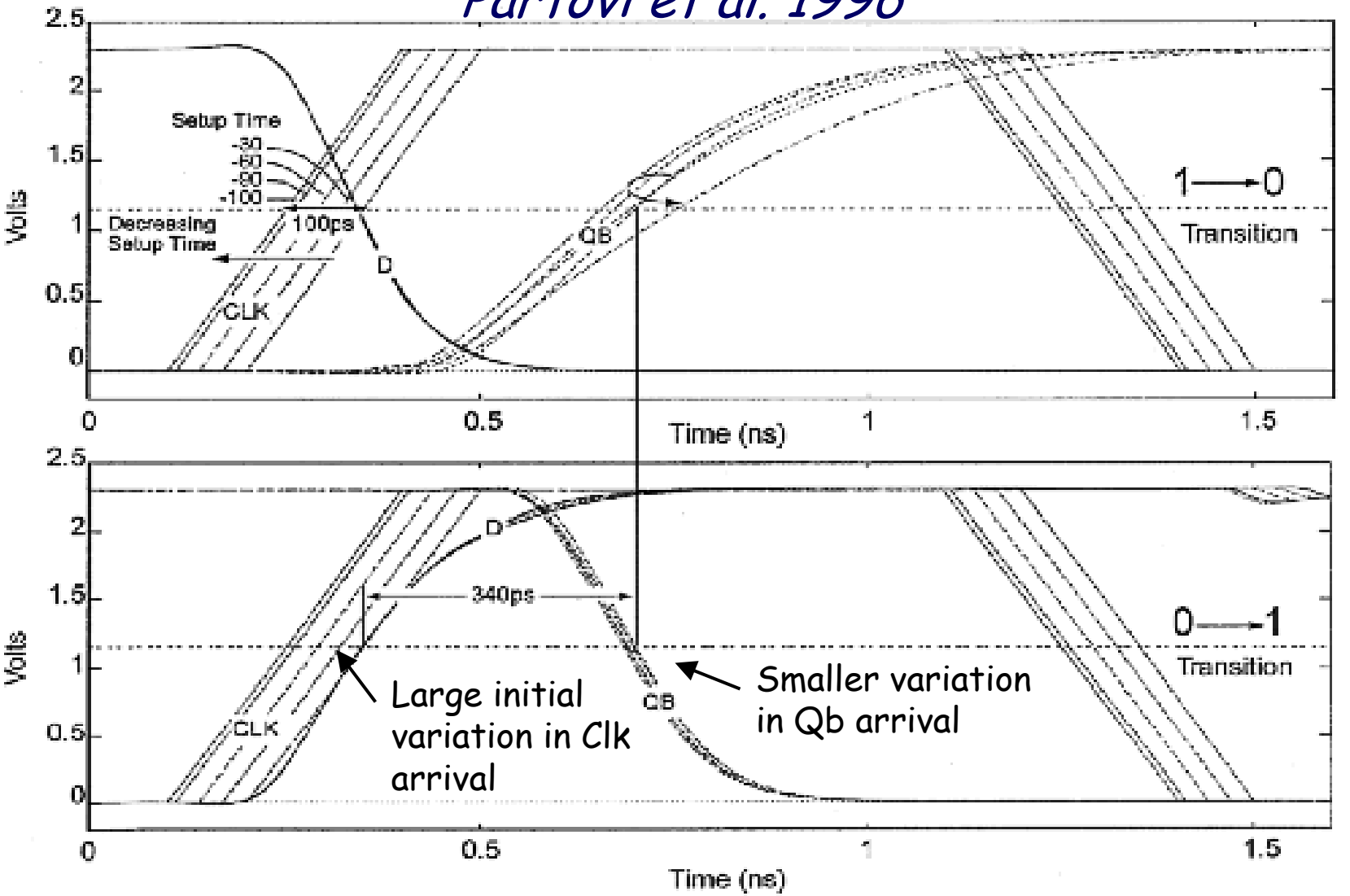
- Jitter
  - *Temporal variation of the clock signal manifested as uncertainty of **consecutive** edges of a periodic clock signal.*
  - It is caused by *temporal* noise events
  - Manifested as:
    - cycle-to-cycle or short-term jitter, t_{JS}
    - long-term jitter, t_{JL}
  - Mainly characteristic of clock generation system
- Skew
  - Time difference between temporally-equivalent or *concurrent edges* of two periodic signals
  - Caused by *spatial* variations in signal propagation
  - Manifests as CSE-to-CSE fluctuation of clock arrival at the same time instance
  - Characteristic of clock distribution system

Clock Uncertainties



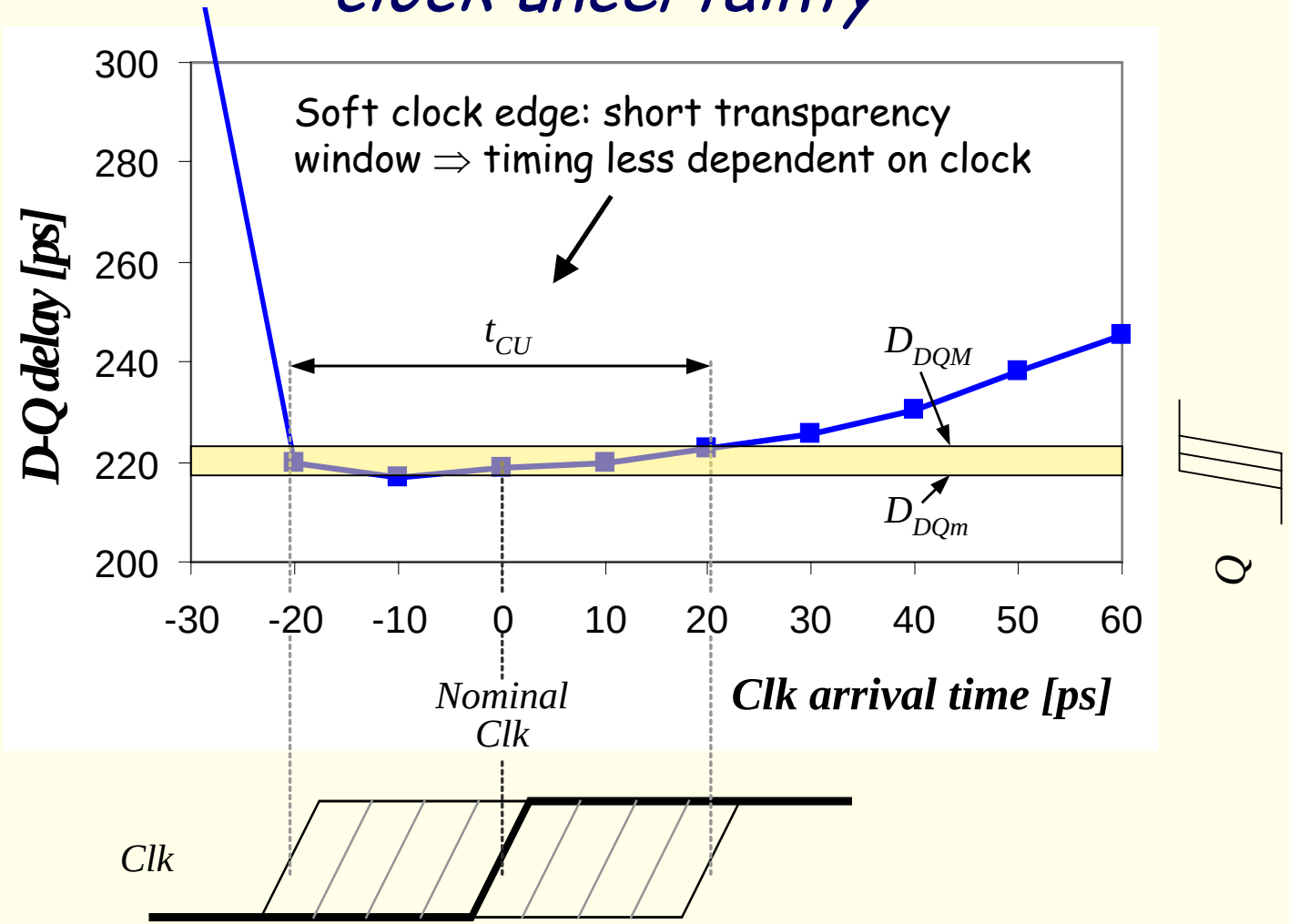
Clock Uncertainty Absorption Using Soft Clock Edge

Output of a flip-flop in the presence of clock jitter: Partovi et al. 1996



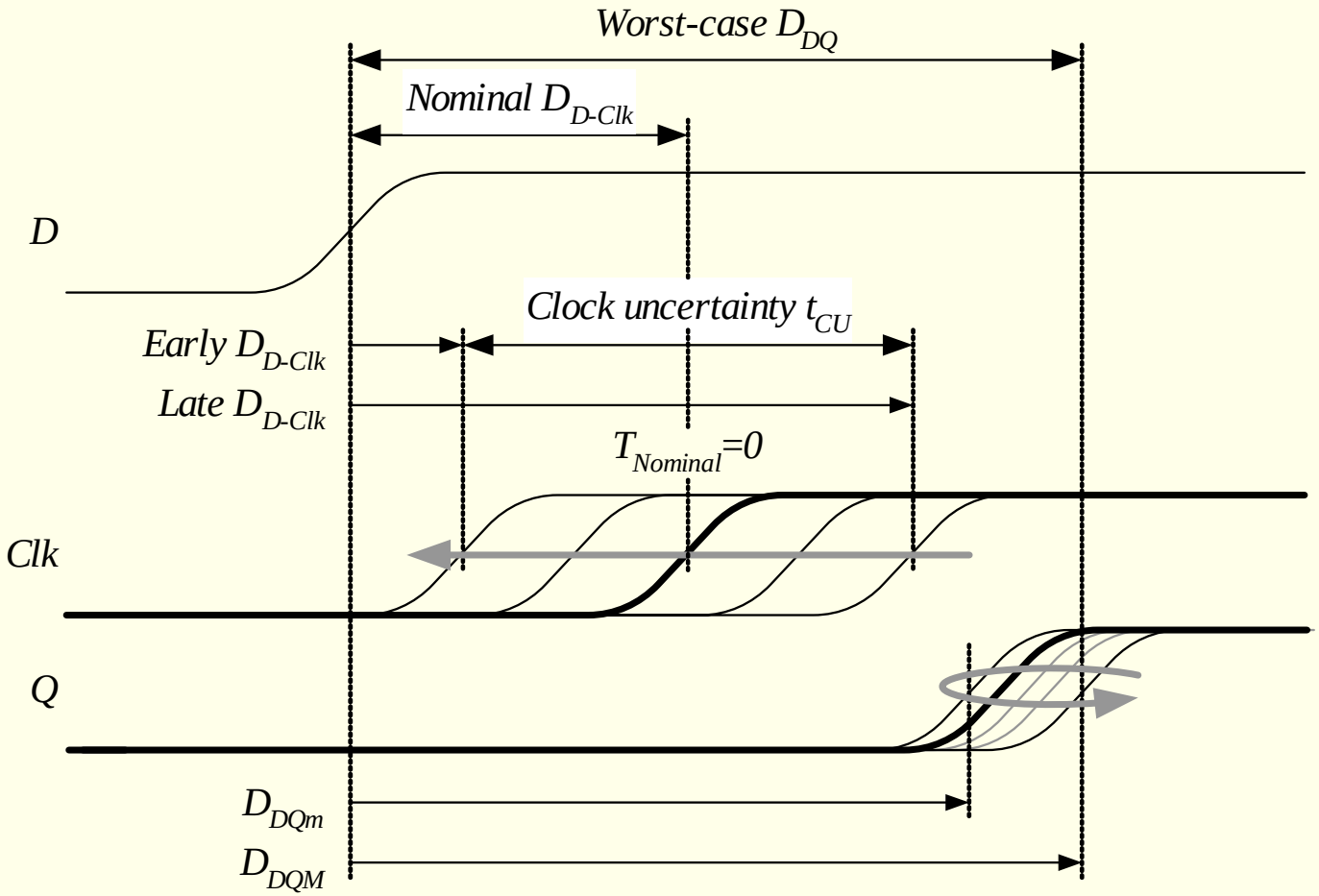
A recent design of a Flip-Flop, controlled by a narrow, locally generated clock pulse, with negative Setup Time exhibits some degree of clock uncertainty absorption.

Data-to-output characteristics in the presence of clock uncertainty



Data-to-Output Delay versus *Clock Arrival Time* when the data arrival time is constant. When no clock uncertainties are present, the clock is scheduled to arrive so that *D-Q* delay (t_{DQm}) is smallest, in order to minimize the CSE overhead.

Dependence of data-to-output delay on clock arrival



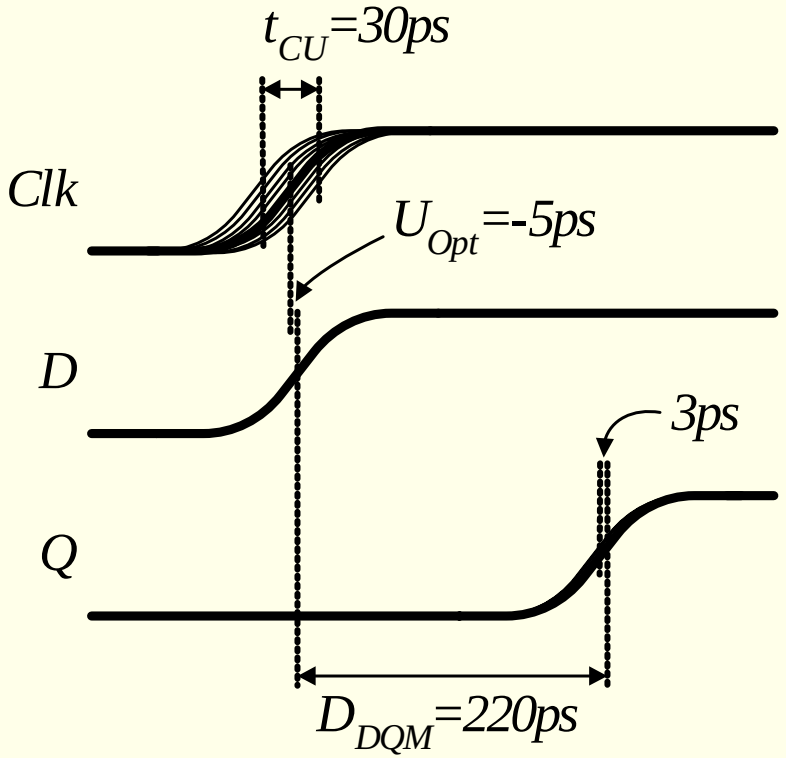
The key role of a CSE is to minimize the propagation of clock uncertainty to the CSE output:

$$D_{DQM} = \max_{t} \; [D_{DQ}(U_{Opt} + t)], \;\; t \in [-t_{CU}/2, \; t_{CU}/2]$$

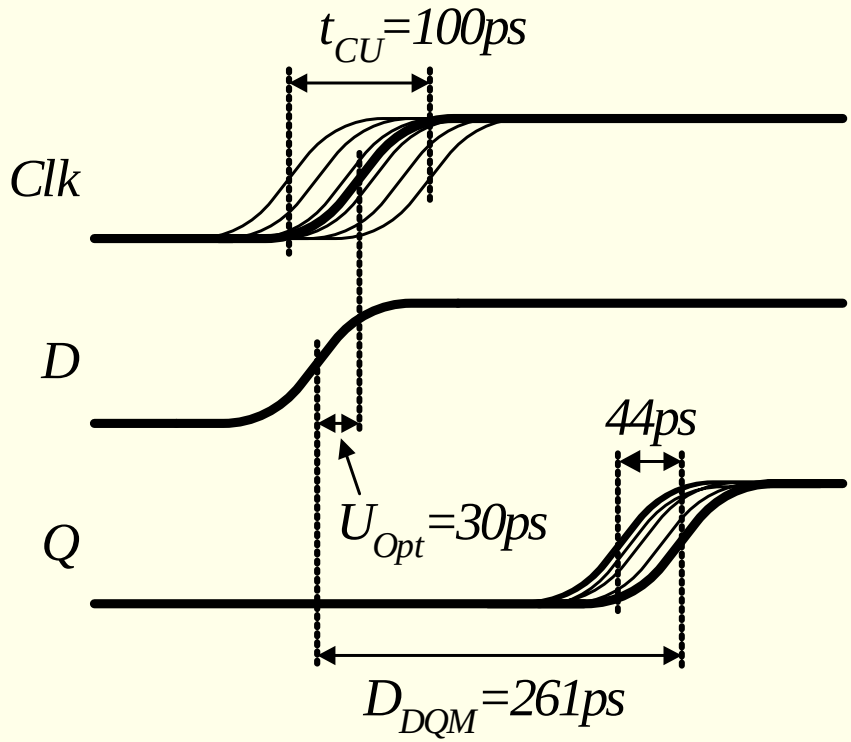
Timing Analysis with Clock Uncertainty Absorption

Total delay versus clock uncertainty

$$D_{DQm} + (1 - \alpha_{CU})t_{CU} + D_{LM} \leq P$$



(a) t_{CU}=30ps (a_{CU}=90%)

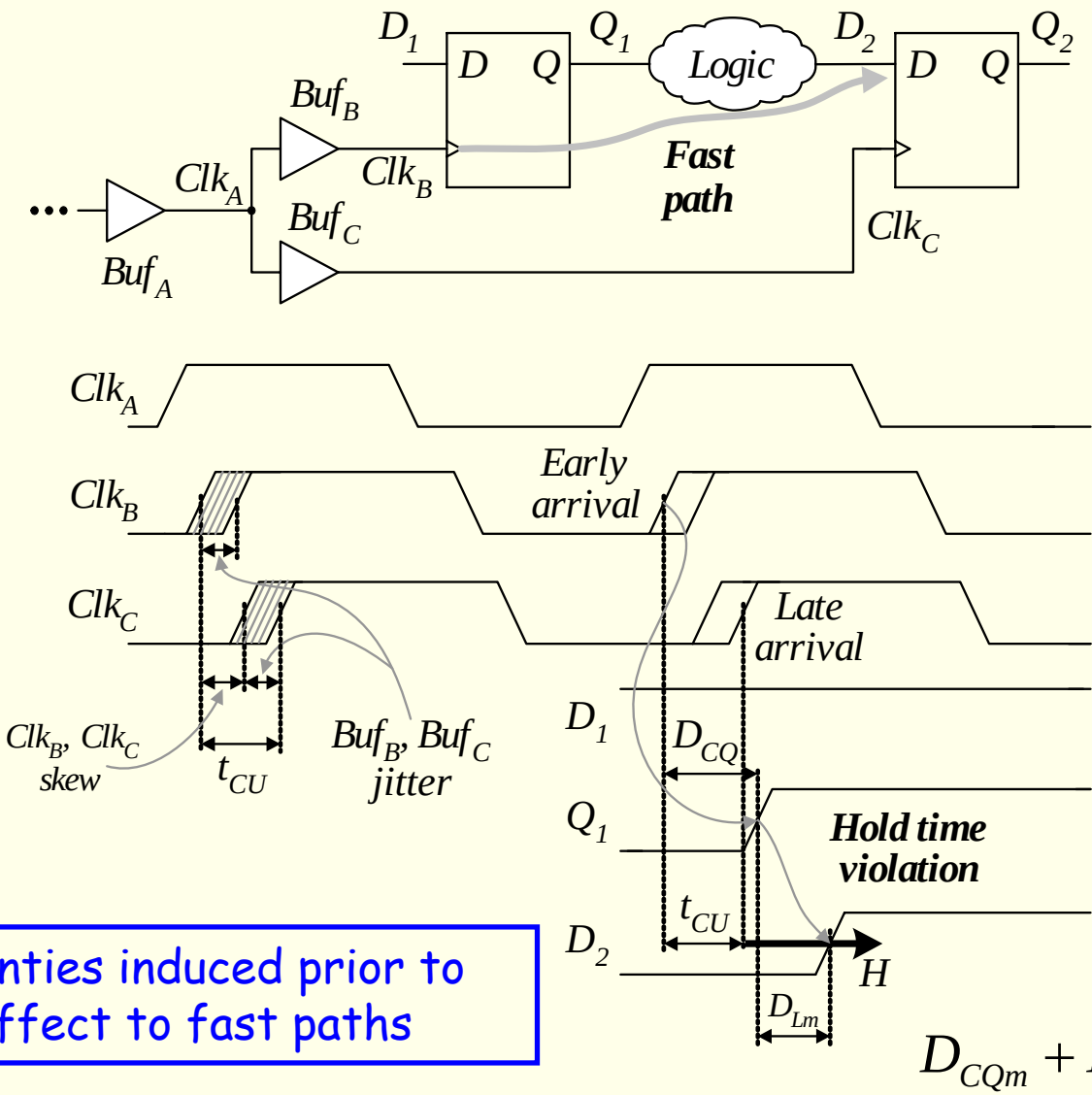


(b) t_{CU}=100ps (a_{CU}=56%)

We formulate *clock uncertainty absorption* α_{CU} of a storage element as the portion of the total clock uncertainty not reflected at the output:

$$\alpha_{CU} = \frac{t_{CU} - (D_{DQM} - D_{DQm})}{t_{CU}} = 1 - \frac{\Delta D_{DQ}}{t_{CU}}$$

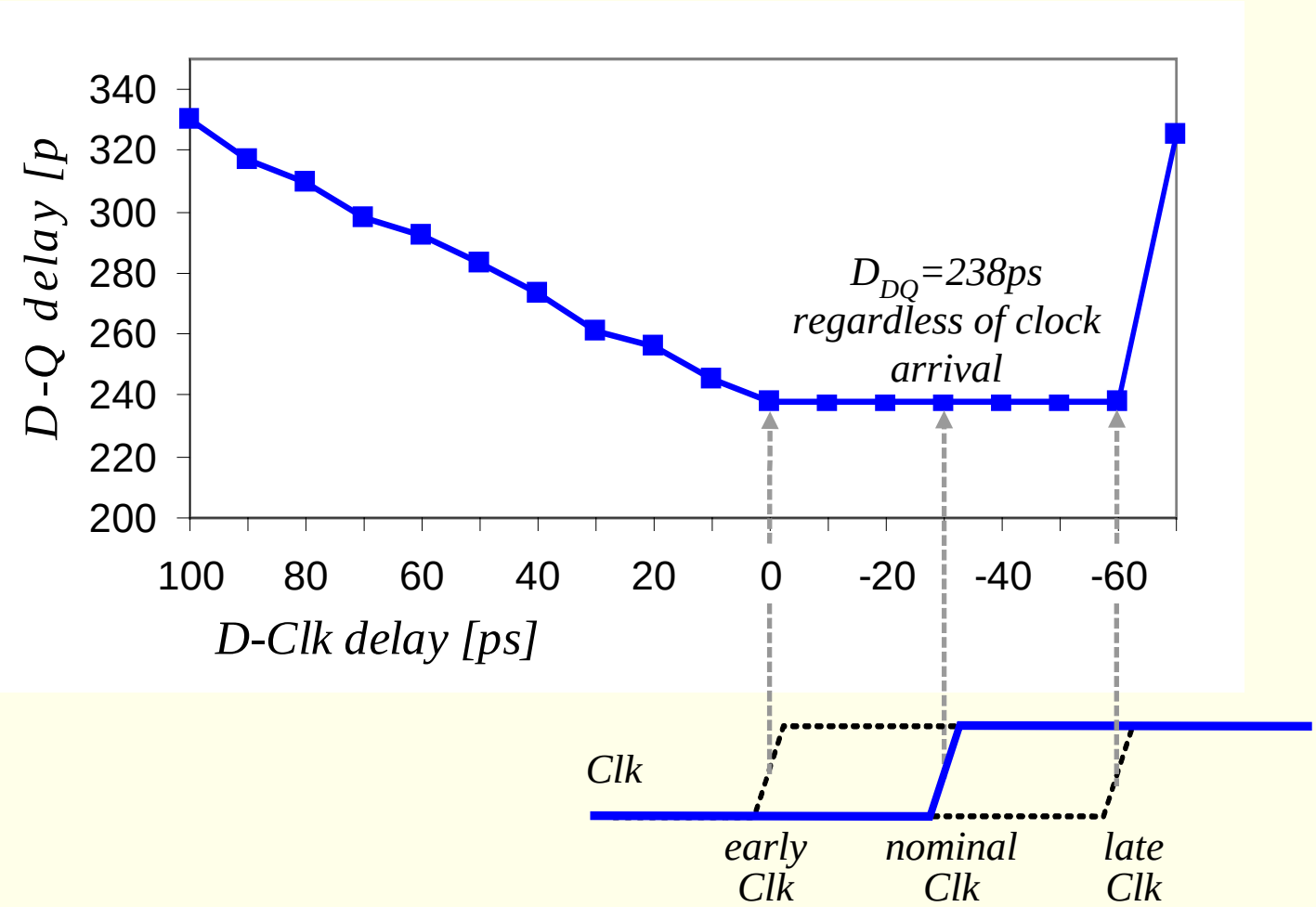
Critical race in the presence of clock uncertainty



Clock uncertainties induced prior to Clk_A have no effect to fast paths

$$D_{CQm} + D_{Lm} \geq H + t_{CU}$$

Idealized D-Q delay characteristic as a function of clock arrival



Time Borrowing

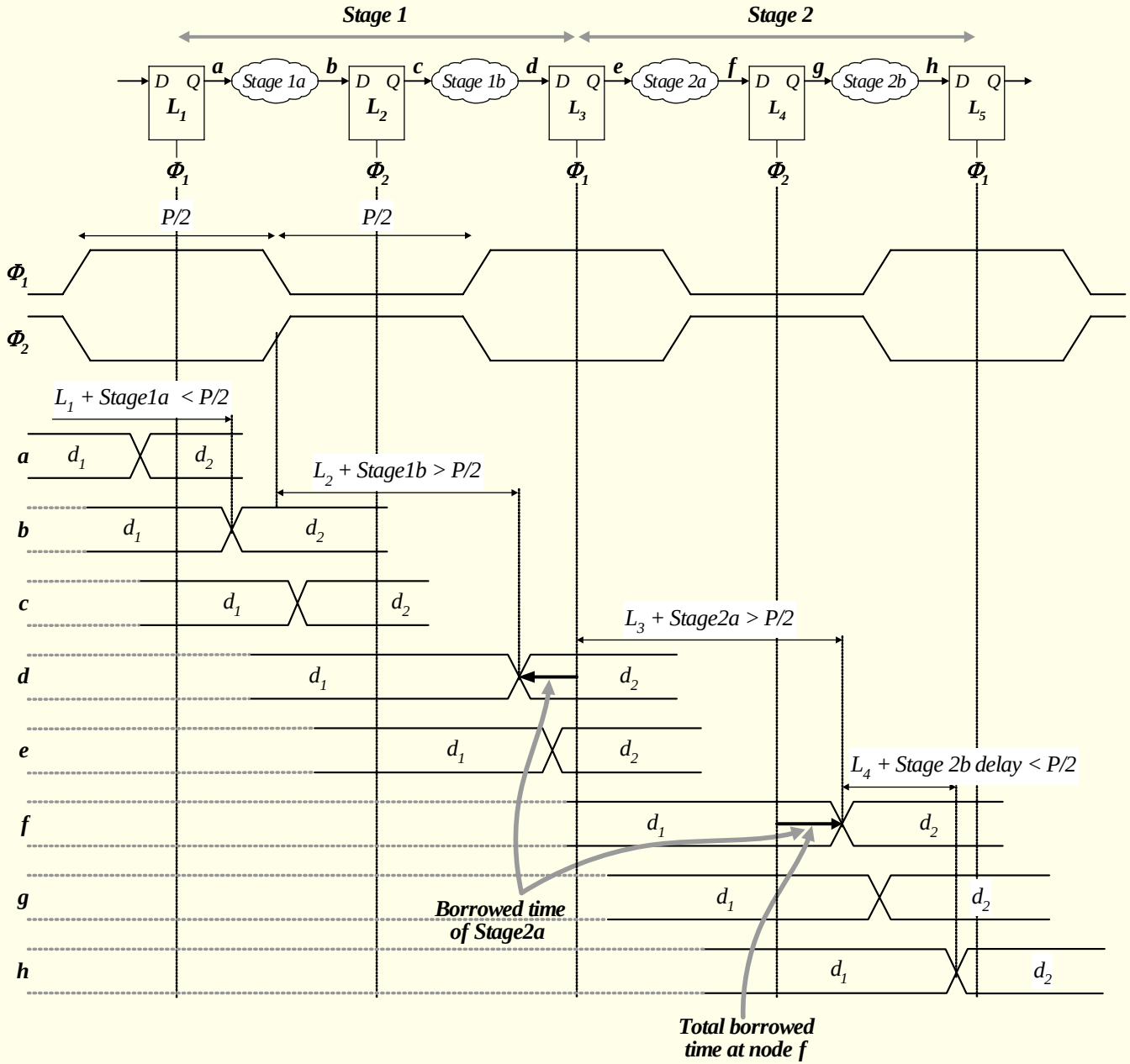
Time Borrowing

Classification:

- Dynamic time borrowing
  - Scheduling data to arrive to CSE when CSE is transparent
    - No "hard" boundaries between stages
  - Occurs in latch-based level sensitive and soft-edge clocking.
- Static time borrowing
  - Inserting delay between clock inputs of the clocked storage elements.
  - Clocks are scheduled to arrive so that the slower paths obtain more time to evaluate, taking away the time from faster paths.
  - It can operate with conventional hard-edge Flip-Flops.
  - Also called *opportunistic skew scheduling*

Dynamic Time Borrowing

Timing of two-phase level-sensitive pipeline with time borrowing



Timing Analysis with Time Borrowing: Late Data Arrival

The minimum clock cycle time of the pipeline is not determined by the delay of the slowest stage in the pipeline. It is rather the average delay of the logic and latches through all stages.

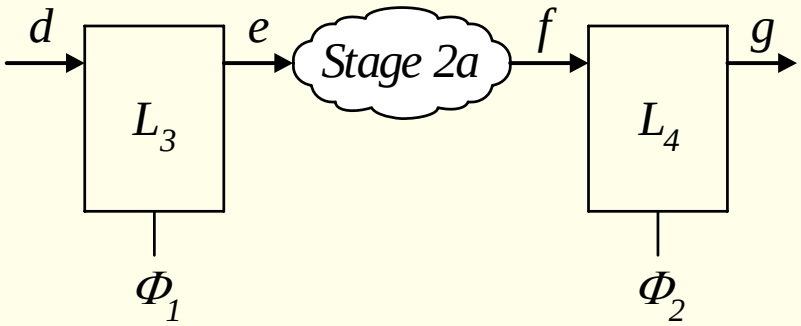
$$P = \frac{1}{N}\sum_{i=1}^{2N}(D_{DQ,i} + D_{Logic,i})$$

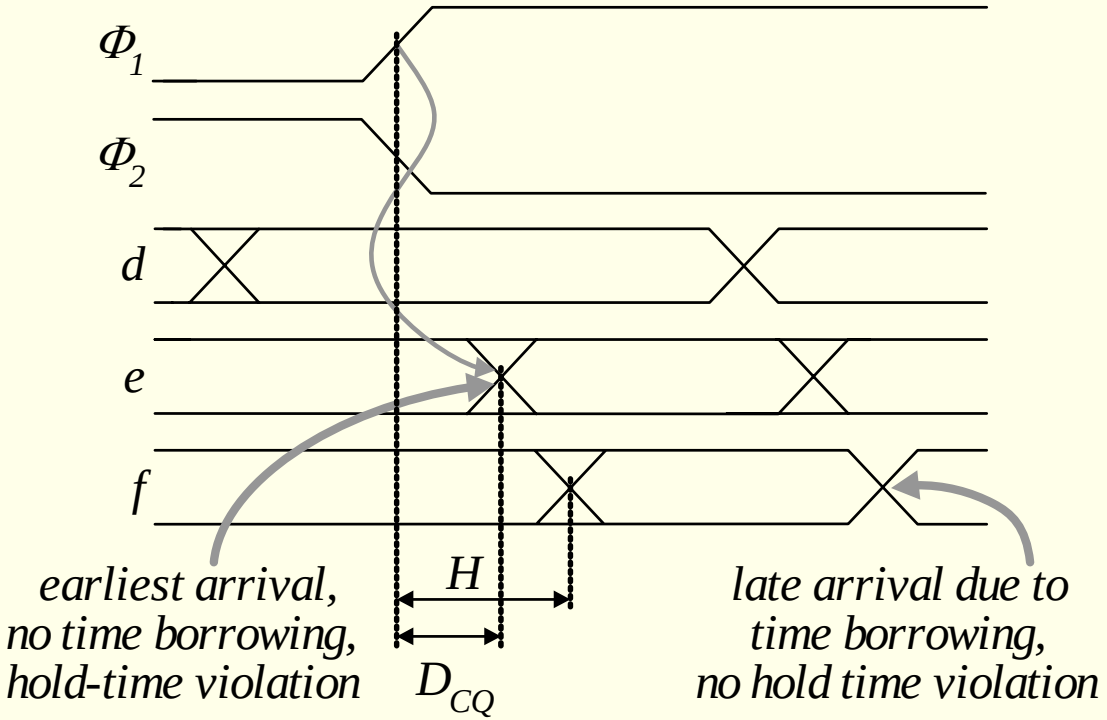
Assumptions:

1) all logic blocks are used in time borrowing,

2) after N stages, the pipeline produces data at the same point in the cycle at which the input data was acquired

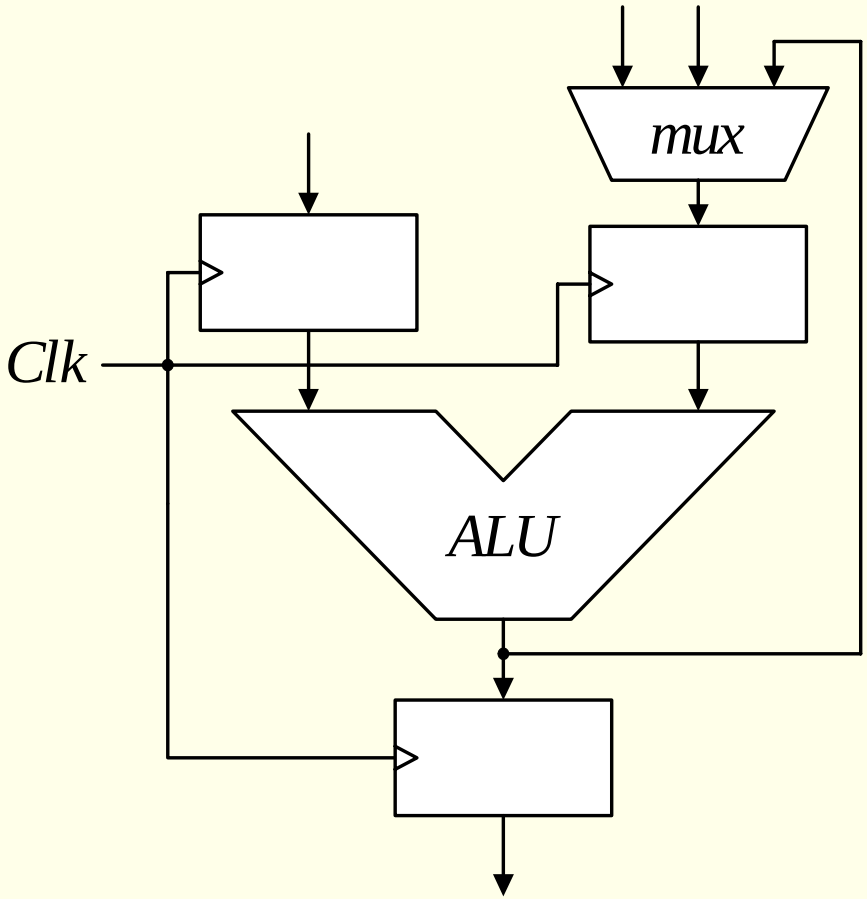
Fast-path hazard





In fast paths, analysis must assume that the data arrives at earliest possible time -> disregard effects of time borrowing

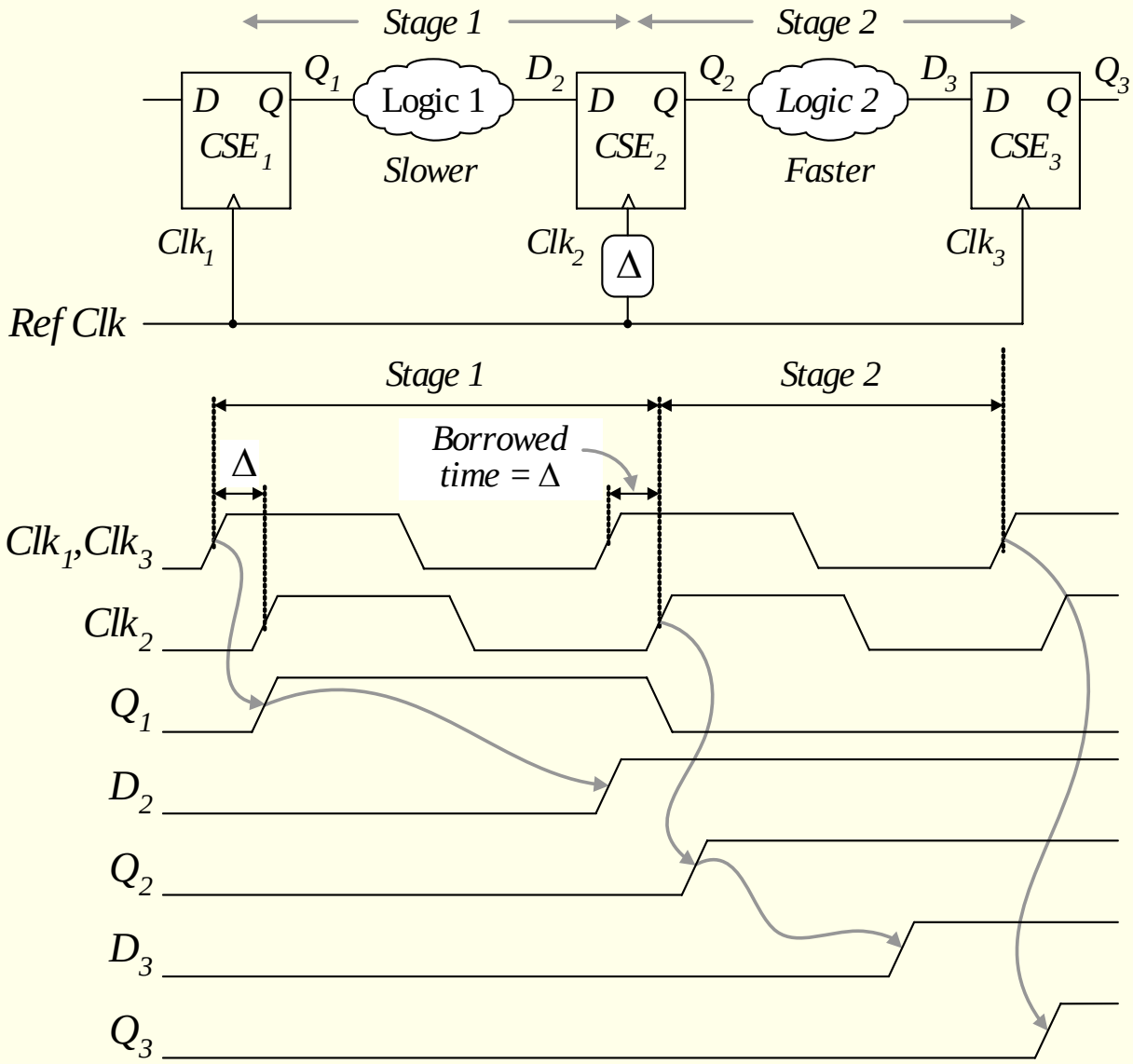
Time borrowing and signal loops



The timing of signals in the loops, should be treated separately.
If the overall propagation delay through the loop occur later with each cycle, it will result in a Setup Time violation.
Any signal loop that borrows time from itself will eventually cause a timing violation.

Static Time Borrowing (Opportunistic Skew Scheduling)

Opportunistic skew scheduling



Opportunistic skew scheduling

Advantages:

- It can operate with conventional Flip-Flops.
- It places fewer constraints onto the circuit design, allowing additional time slack where necessary.

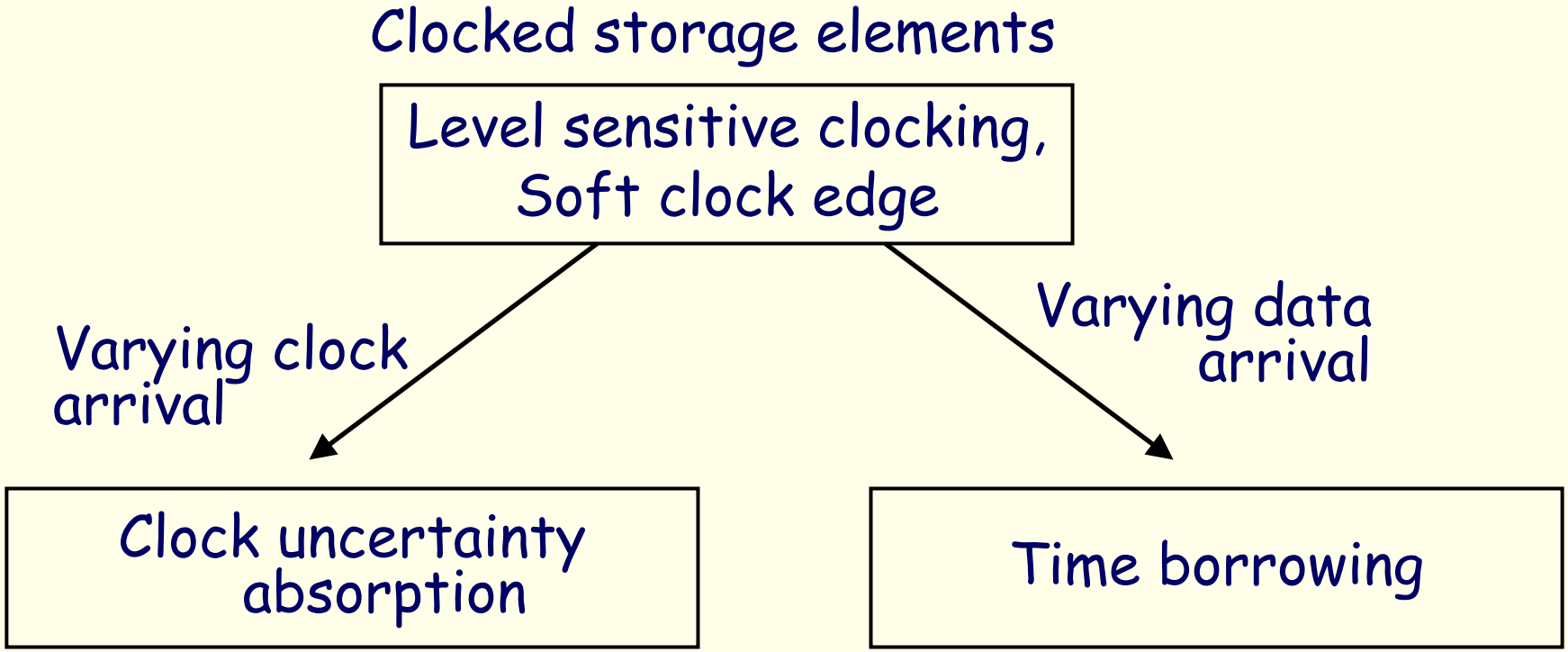
  ⇒ useful in localized critical paths where every improvement directly increases the system clock rate

Disadvantages:

- It increases the complexity of the clock distribution system.
- It is hard to control the inserted delays over process, supply and temperature variations.
- The analysis of clock skew is also complicated in this asymmetric clock distribution network.

  ⇒ impractical on a large-scale level

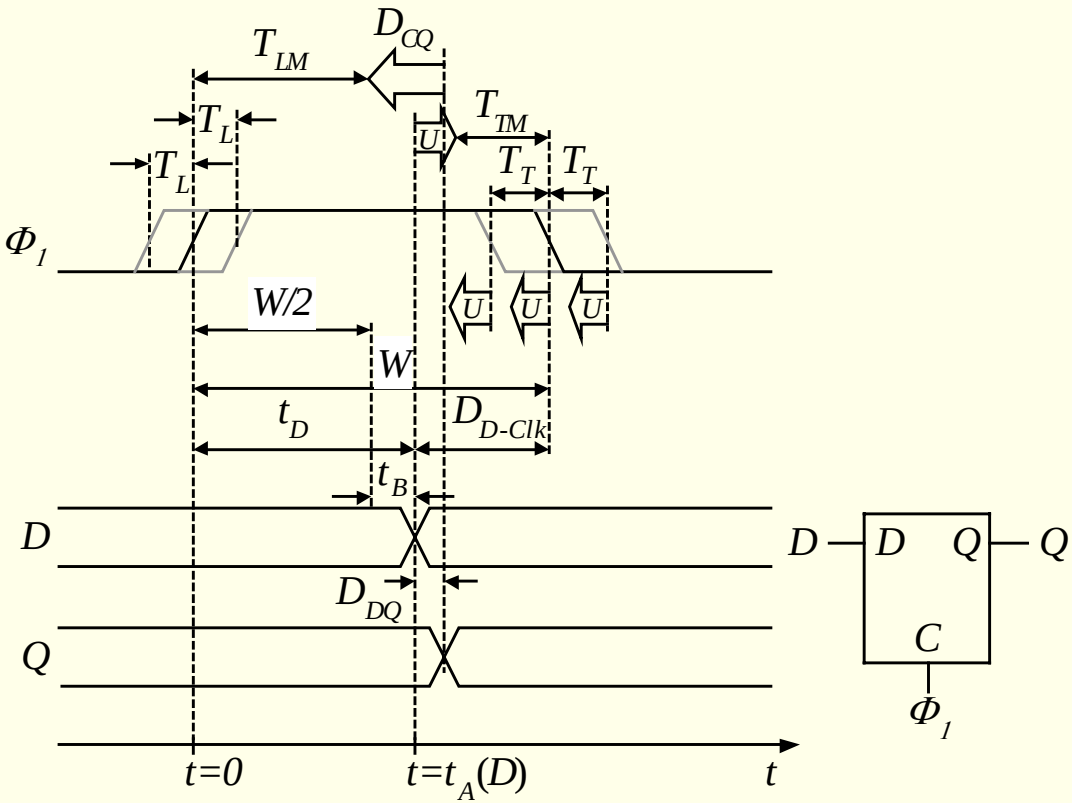
Time Borrowing and Clock Uncertainty



Clock uncertainty absorption and time borrowing exploit the same data transparency property of CSE

Clock Uncertainty Absorption with Level-Sensitive Clocking

Clock uncertainty immunity in single stage



System tolerates up to

$$T_{L,\Phi_1} + T_{T,\Phi_2} \le D_{CQm} + D_{Lm} - V - H$$

before violating hold time

System tolerates up to

$$T_T \le W/2 - t_B - U$$

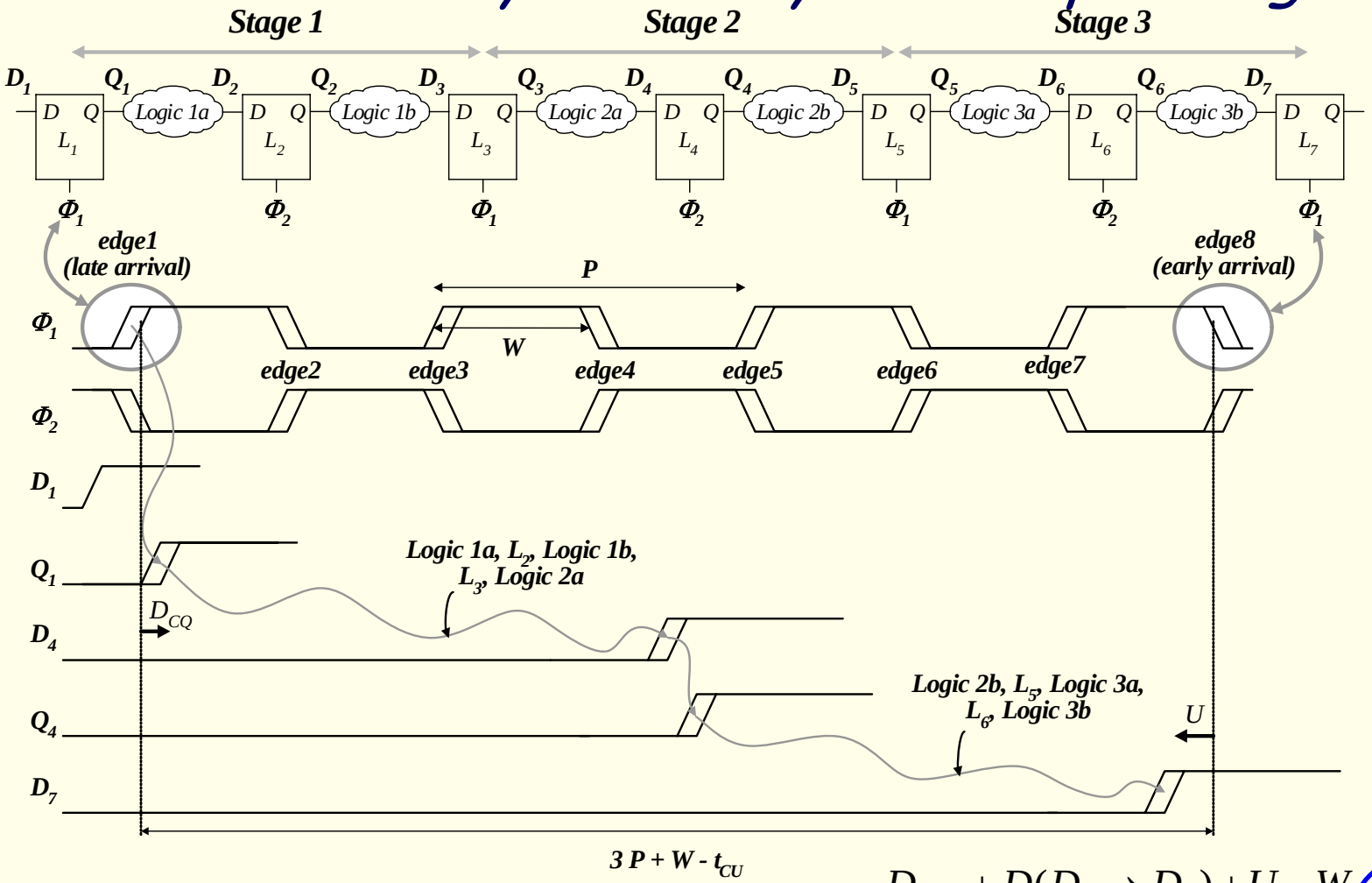
before violating setup time

System tolerates up to

$$T_L \le t_B + D_{DQ} - D_{CQ} + W/2$$

to keep borrowing time

Clock uncertainty immunity in multiple stages



$$t_{CU} + D_{CQ1} + D(D_1 \rightarrow D_7) + U \leq 3P + W \quad \rightarrow \quad P \geq \frac{D_{CQ1} + D(D_1 \rightarrow D_7) + U - W}{3} + \frac{t_{CU}}{3}$$

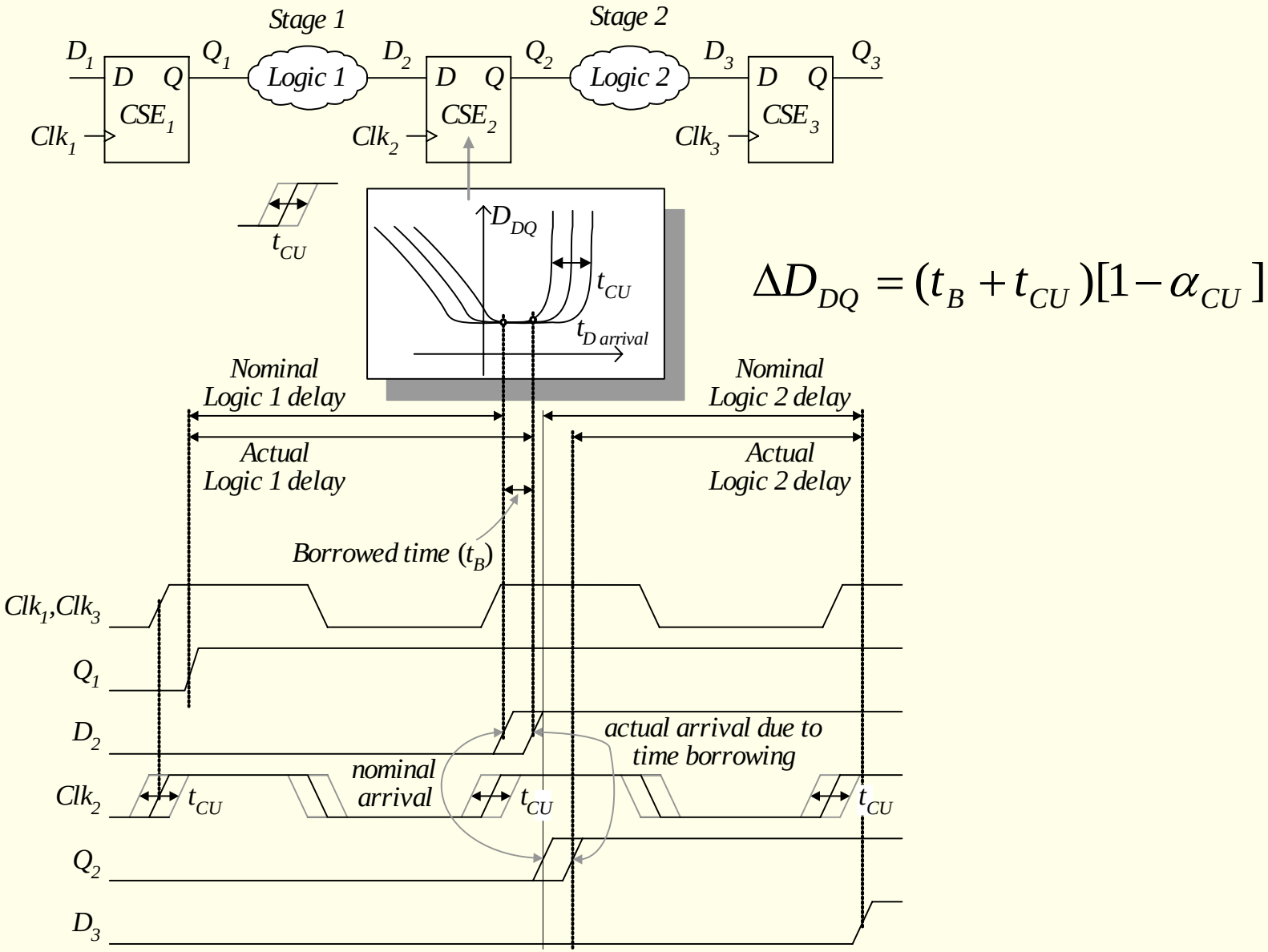
impact of the clock uncertainties reduced over multiple stages

Summary: Effects of clock uncertainties to a system with level-sensitive clocking

- Decreasing of the margins for time borrowing.
- The pipeline absorbs the uncertainties for the data that arrives during the transparency period of the Latch.
- The effect of the uncertainties is reduced to an average uncertainty over all stages in the path.

Soft-Edge Sensitive Clocking

Time borrowing with uncertainty-absorbing clocked storage elements



$$\Delta D_{DQ} = (t_B + t_{CU})[1 - \alpha_{CU}]$$

Conclusion

- High-performance CSE requirements:
  - Speed
  - Clock uncertainty absorption $\Rightarrow$ to accommodate increasing effect of clock skew and jitter
  - Time borrowing $\Rightarrow$ to eliminate effects of imbalanced stage delays
- Essential circuit technique: eliminate hard edges in critical paths
- Flip-flops with soft clock edge, level-sensitive latches become preferred choice of CSE
- Clock uncertainty absorption capability can be traded for time borrowing