Digital System Clocking:

High-Performance and Low-Power Aspects

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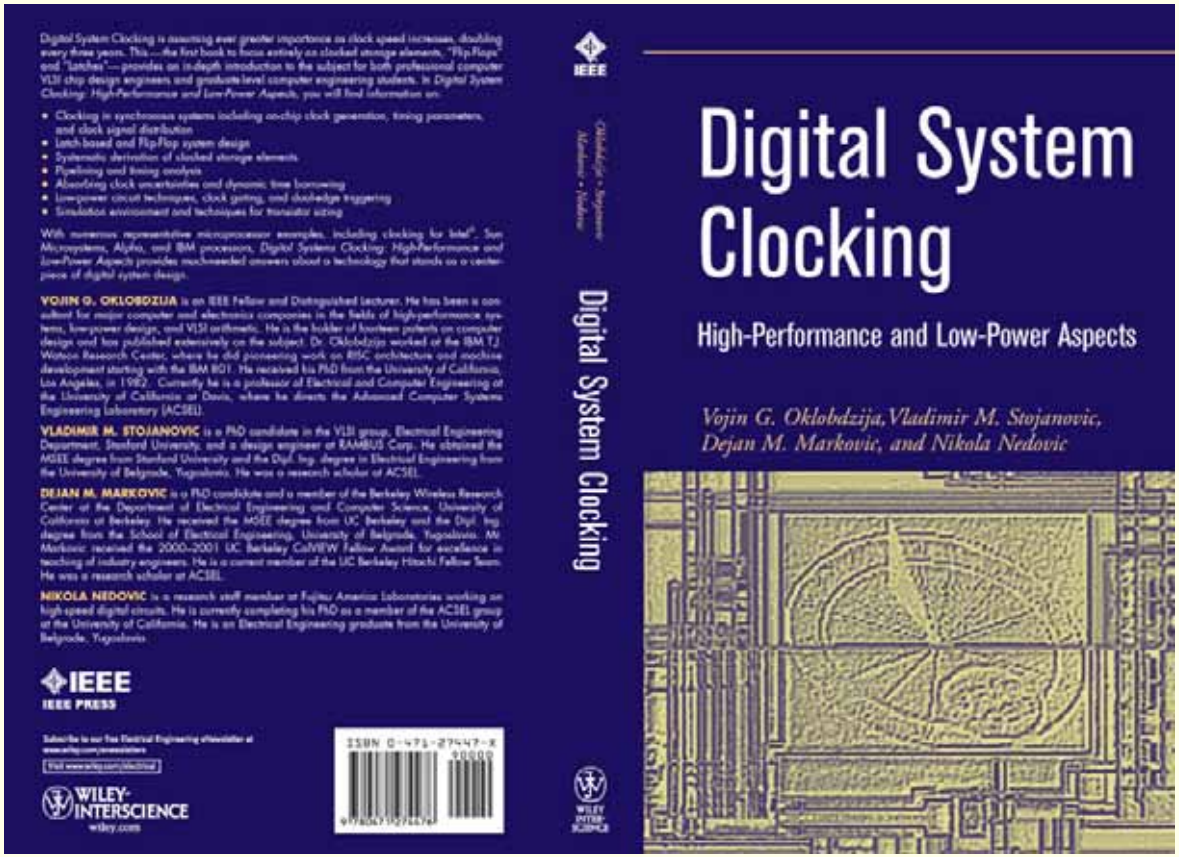
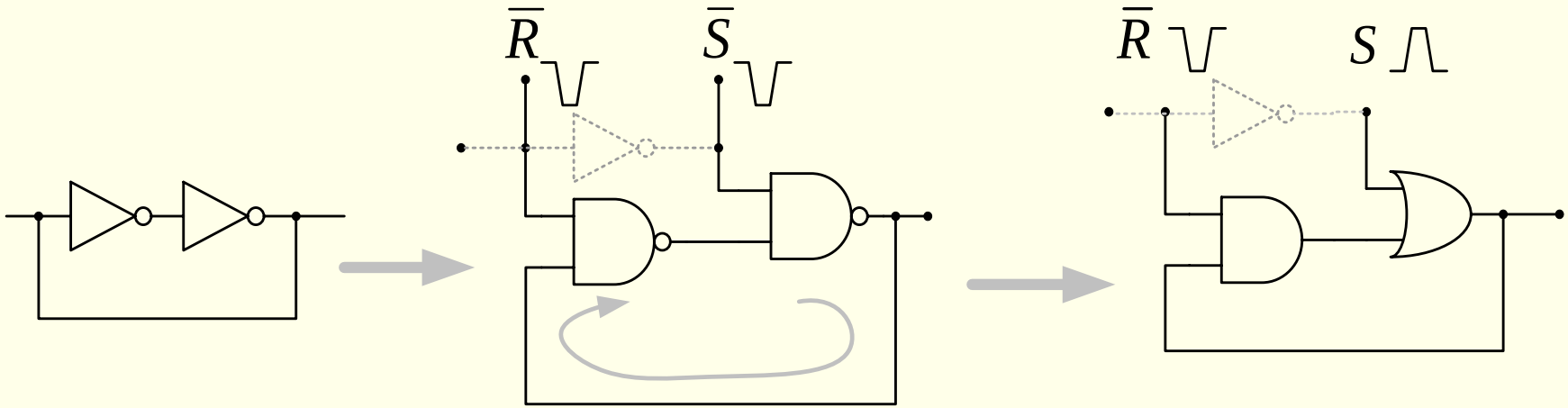
Chapter 2: Clocked Storage Elements Operation



Wiley-Interscience and IEEE Press, January 2003

Evolution of a Latch :

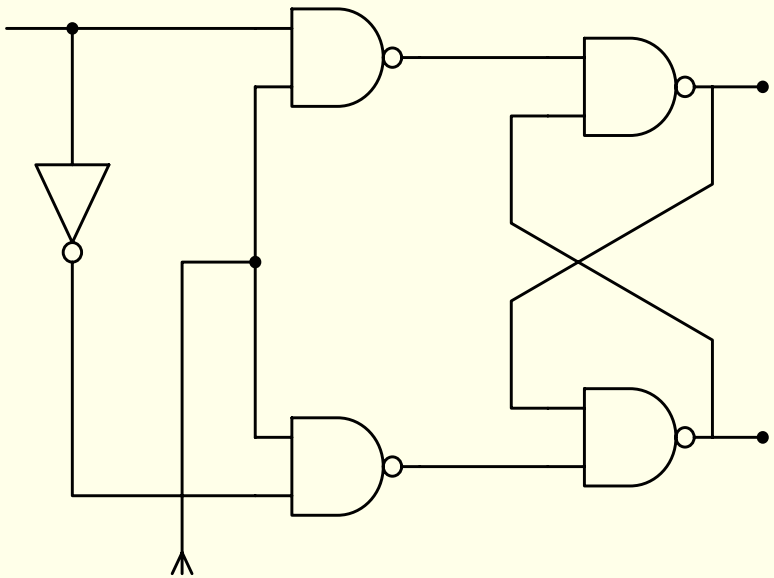


(a) keeper; information is latched

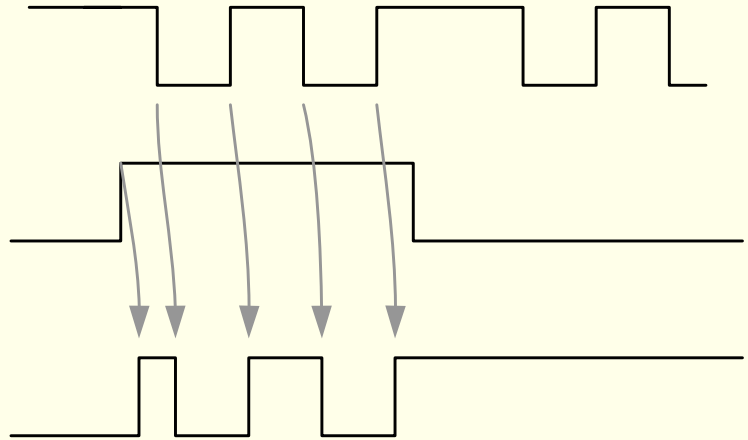
(b) S-R latch; information can be modified

(c) S-o-P latch; S-R latch that can implement a function – IMPORTANT !

Adding Clock Control to a Latch



(a)

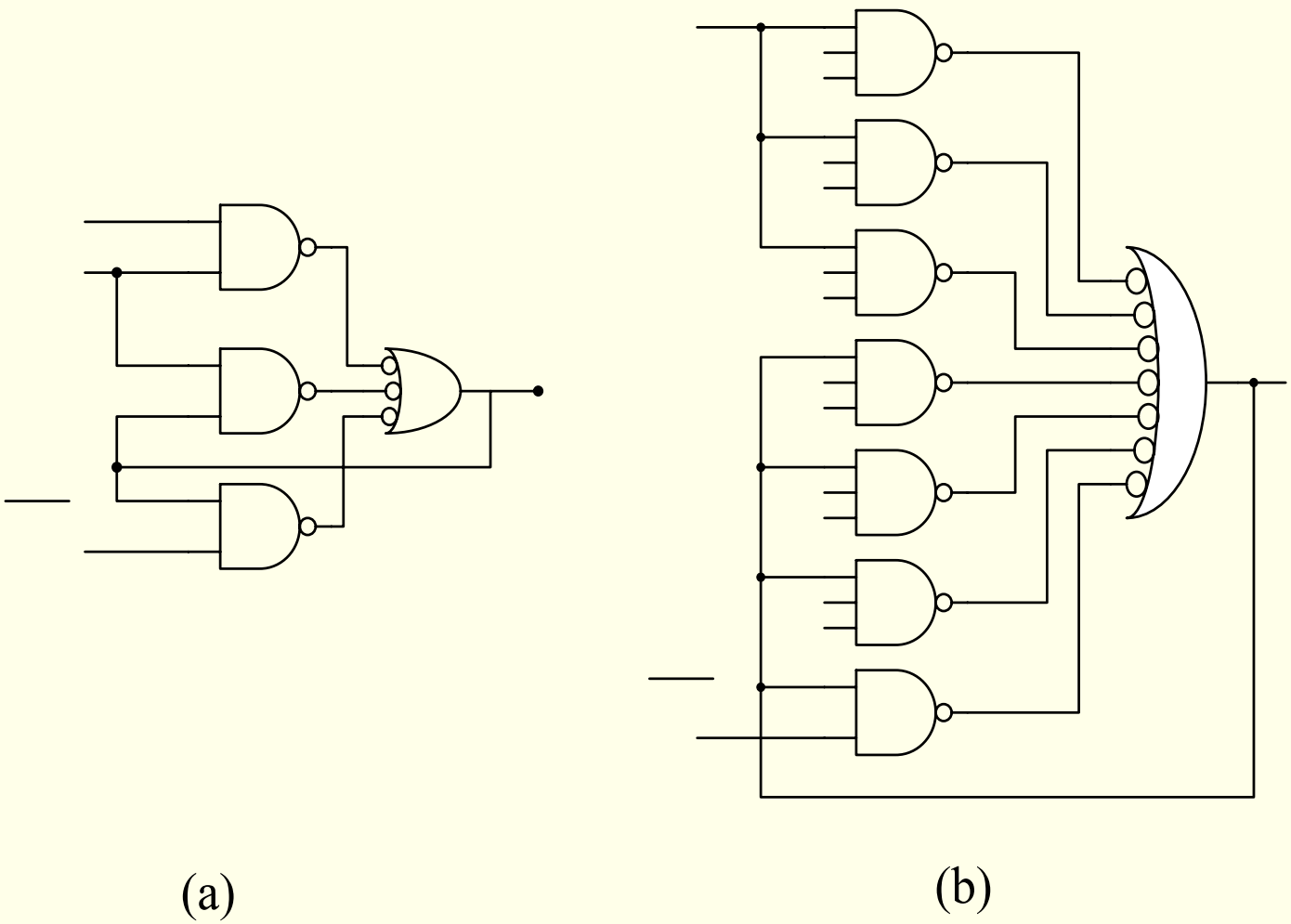


(b)

Latching can be done only when clock is active, otherwise no change is allowed:

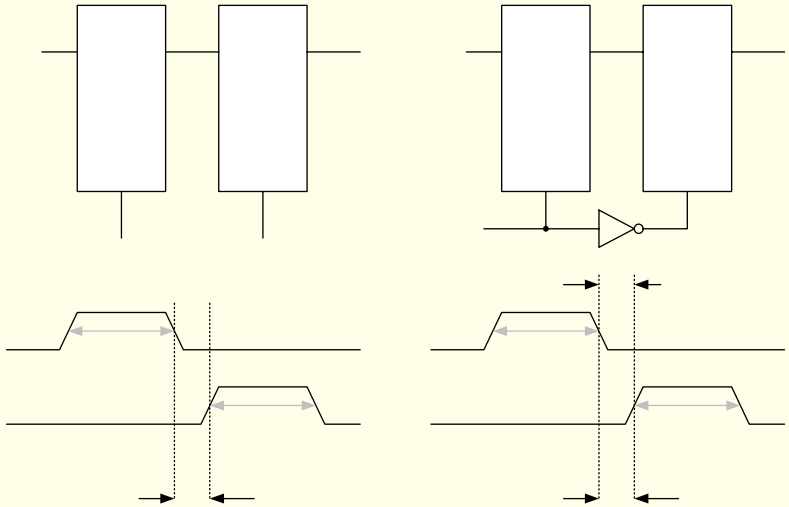
(a) Clocked D-latch; (b) timing diagram of clocked D-latch

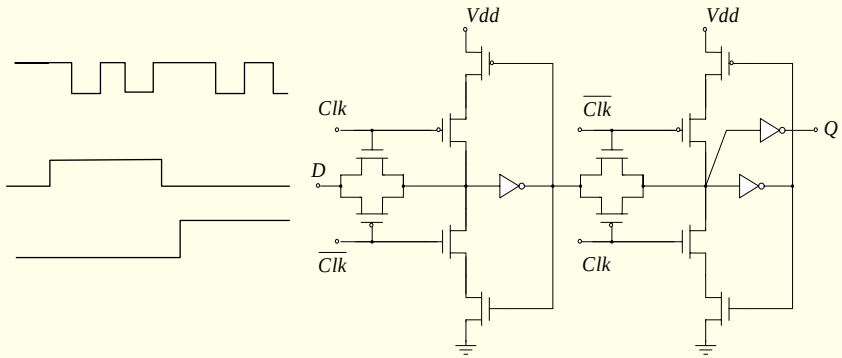
Importance of Latch S-o-P Configuration



(a) Basic Earl's Latch; (b) Implementing the Carry function

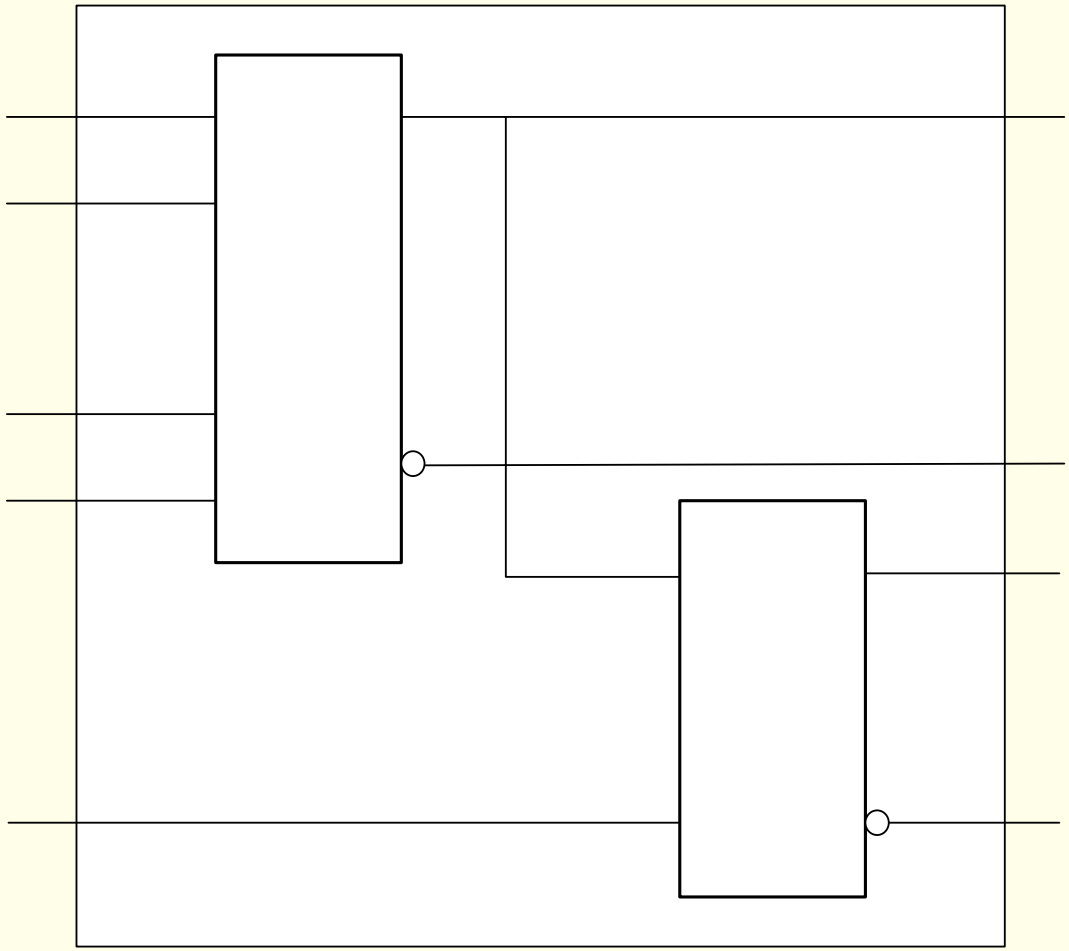
Master-Slave Latch





(a) non-overlapping clocks; (b) single external clock; (c) timing diagram; (d) PowerPC 603 MS Latch (Gerosa, JSSC 12/94), Copyright © 1994 IEEE

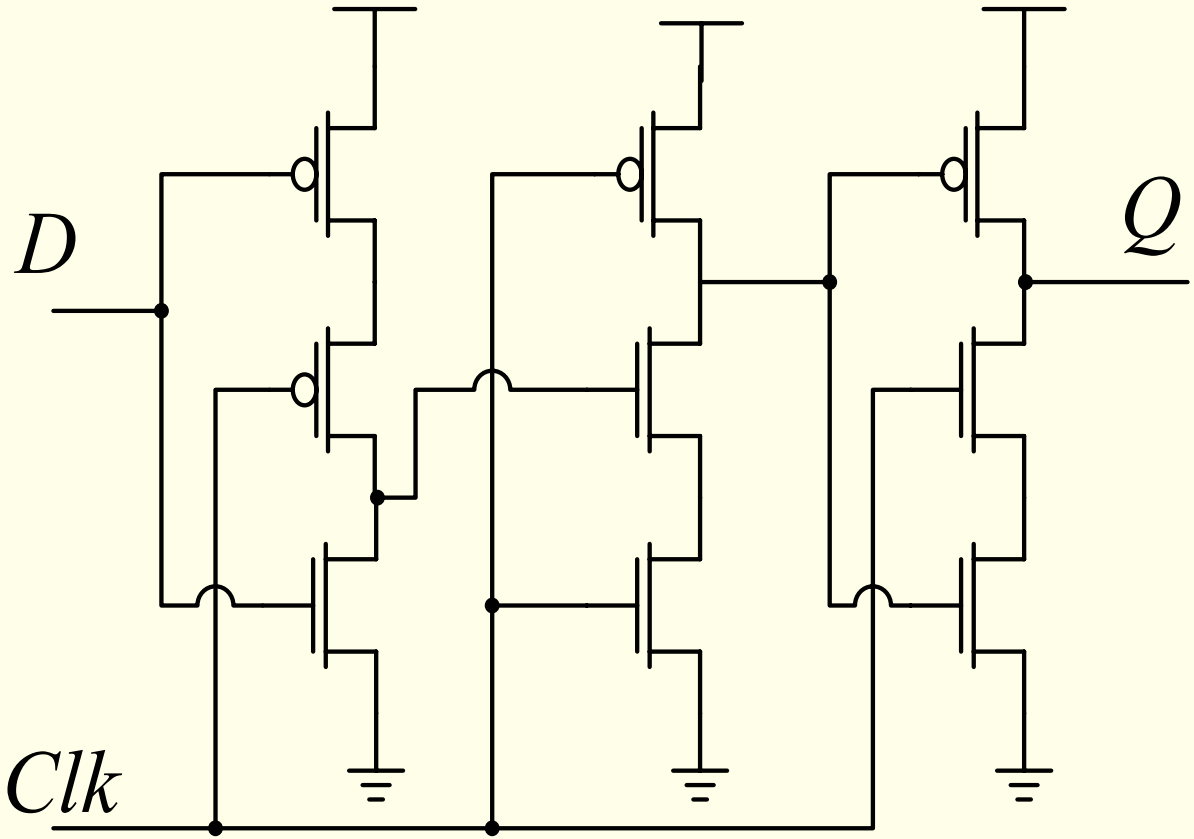
IBM LSSD Compatible Clocked Storage Element



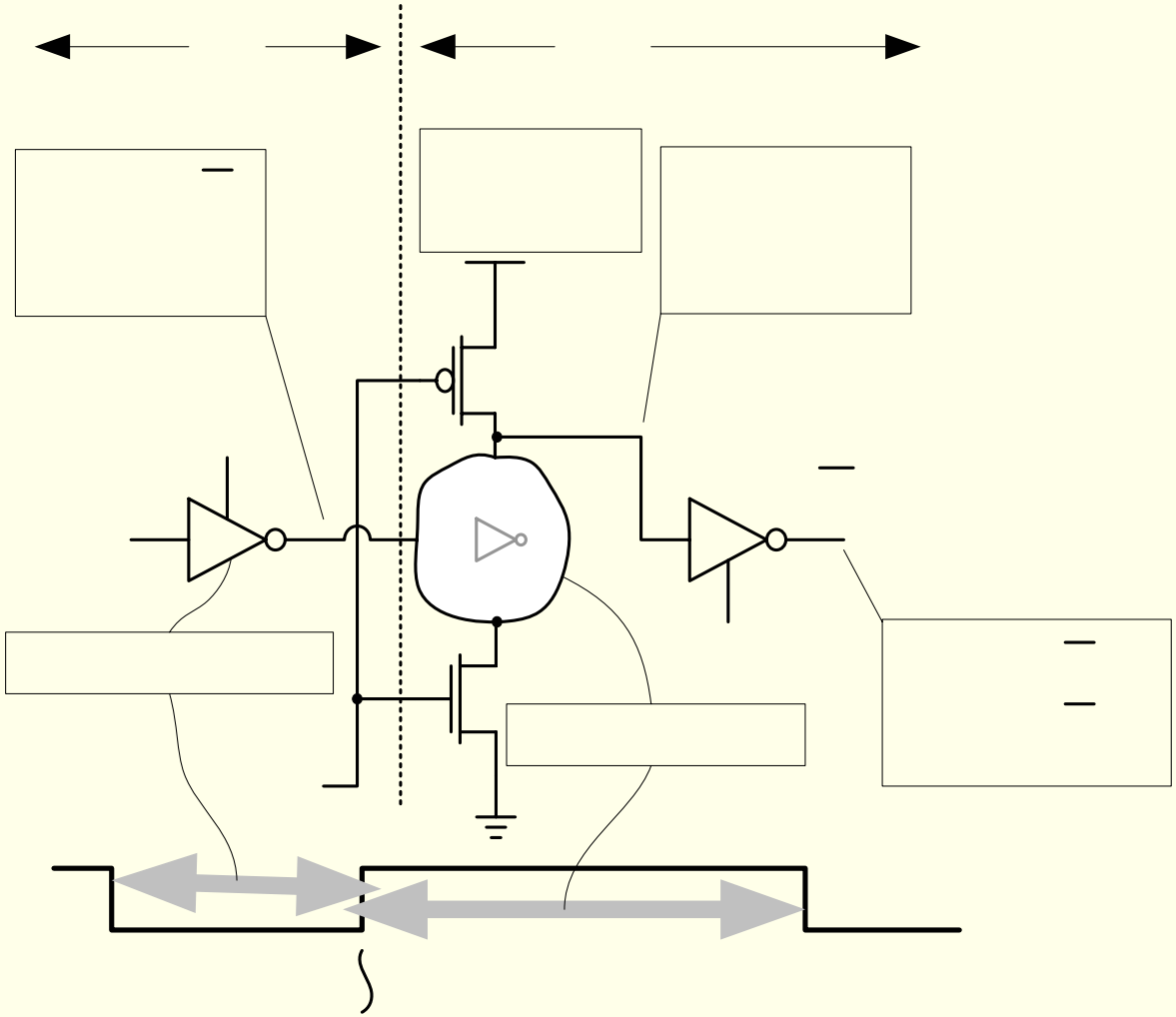
System Data D

True-single-phase-clock (TSPC) M-S latch

Yuan and Svenson (1989), Copyright © 1989 IEEE

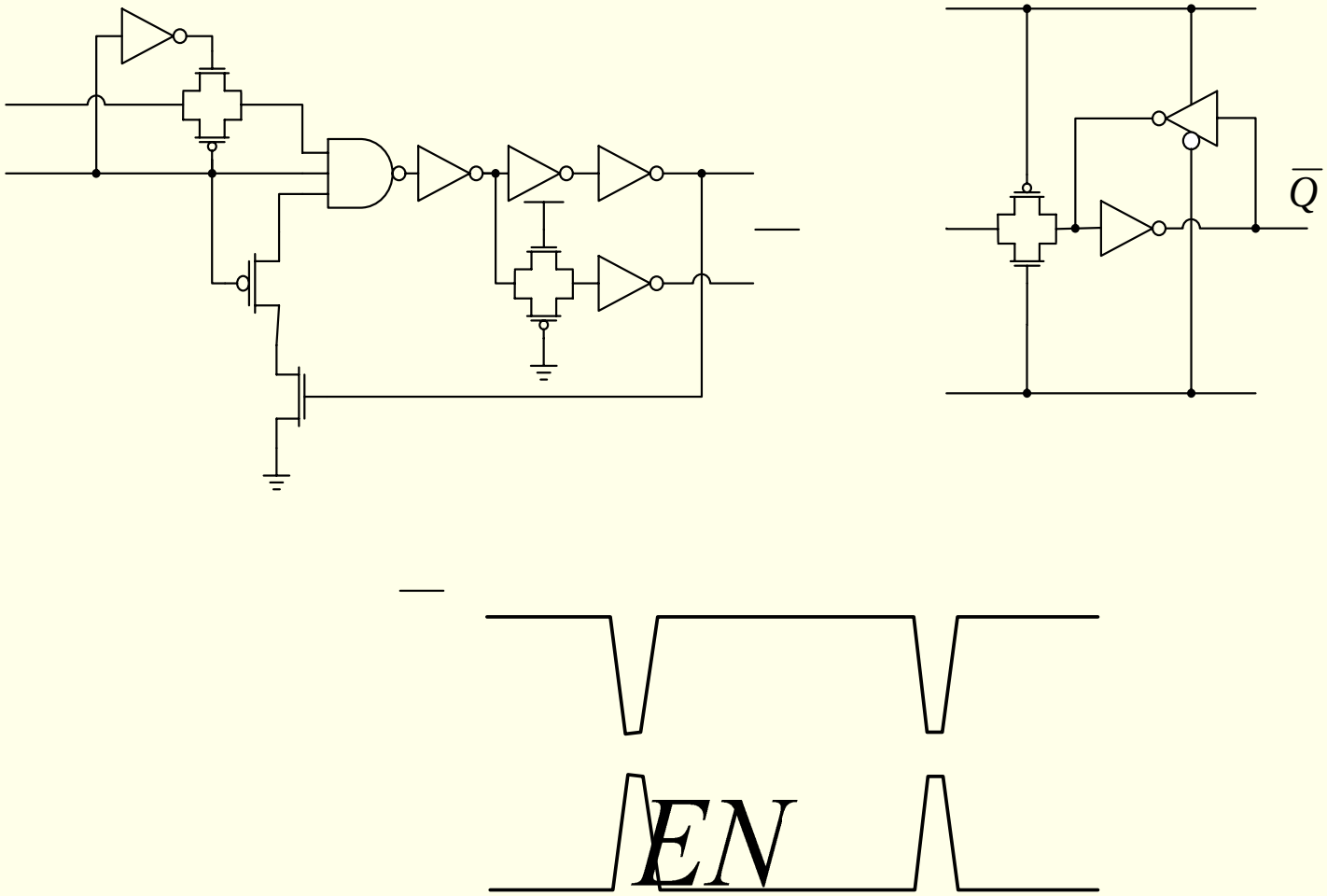


TSPC M-S Latch Operation



Pulse latch

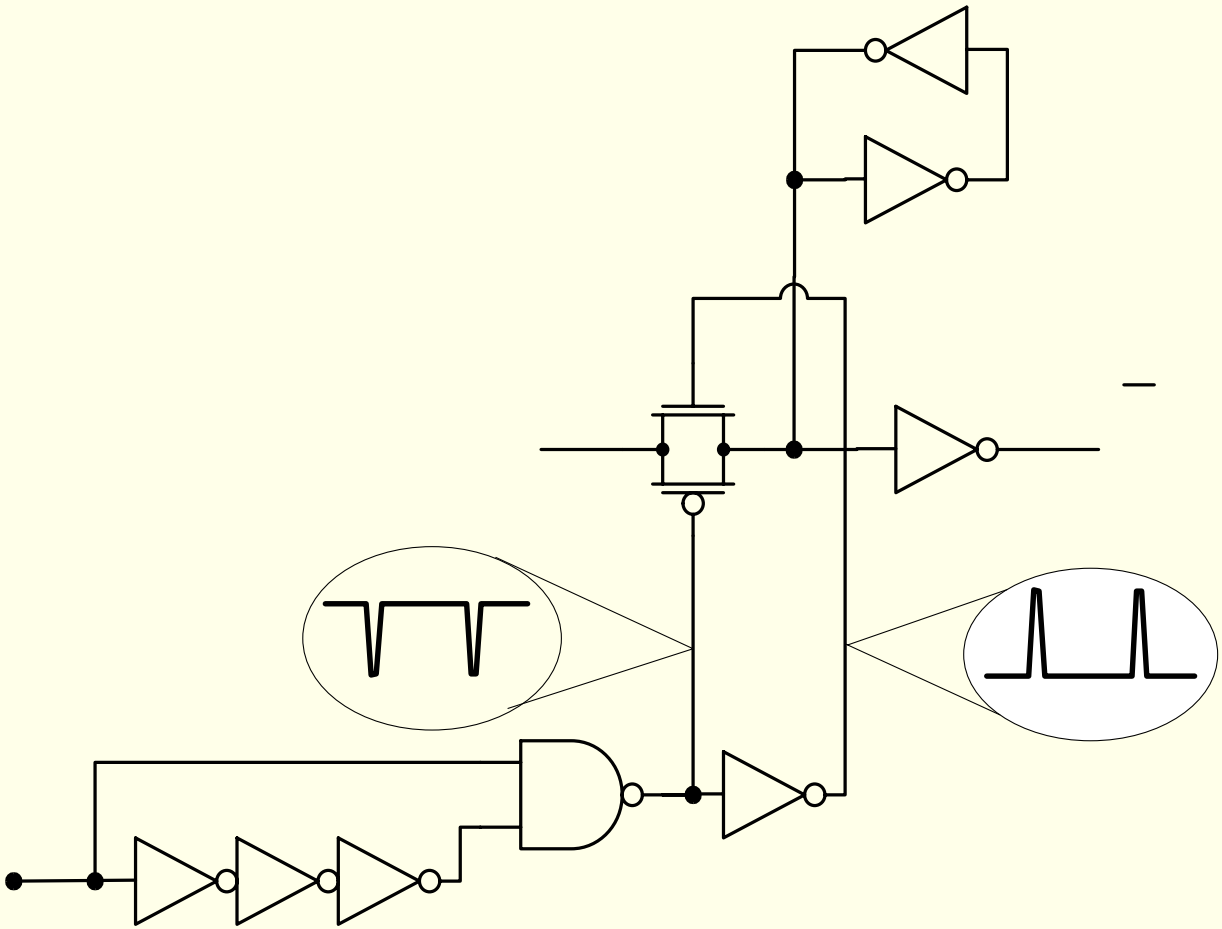
(Kozu at al. 1996) Copyright © 1996 IEEE



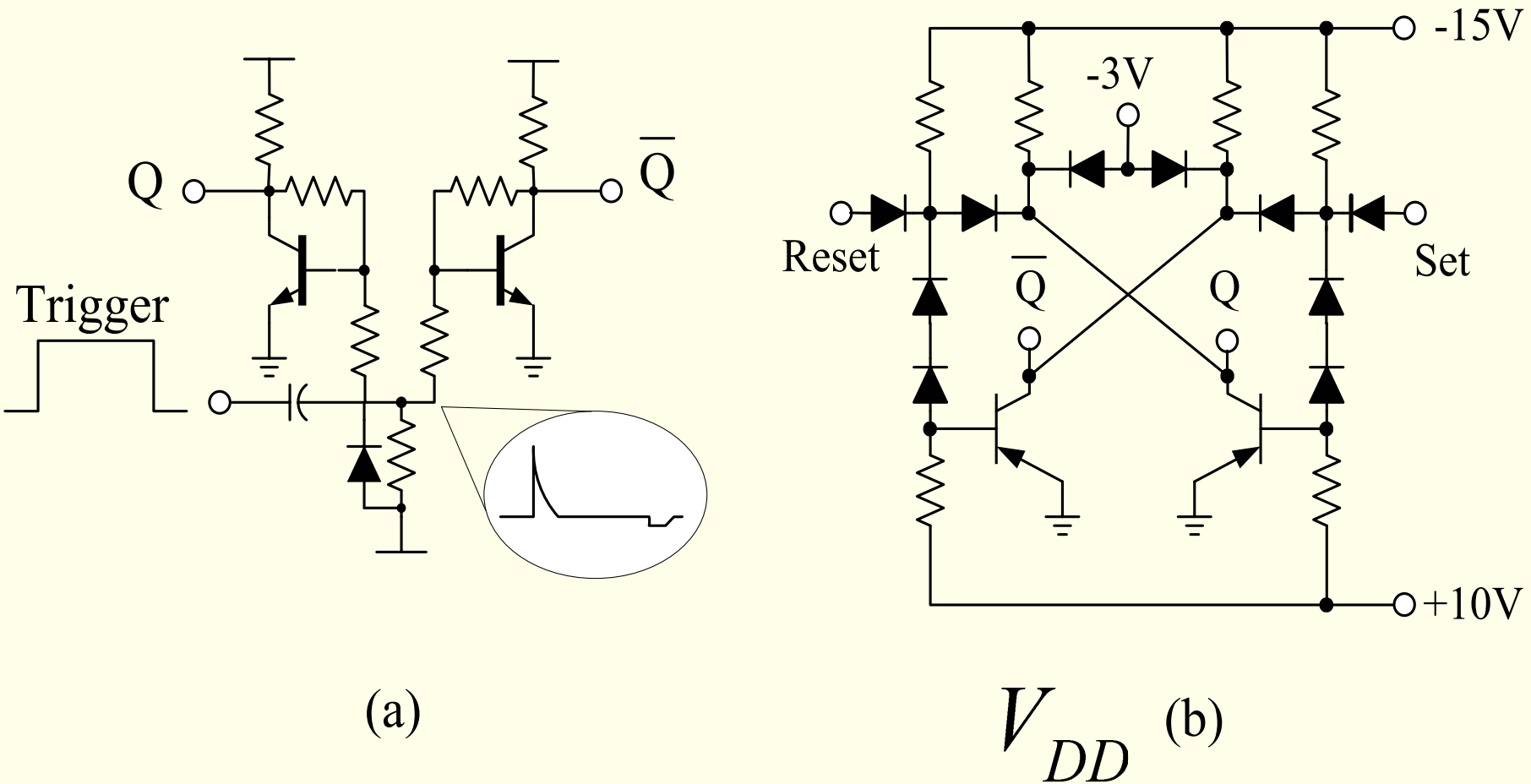
(a) local clock generator; (b) single latch; (c) clock signals

Pulse latch: Intel's explicit pulsed latch

(Tschanz at al. 2001), Copyright © 2001 IEEE

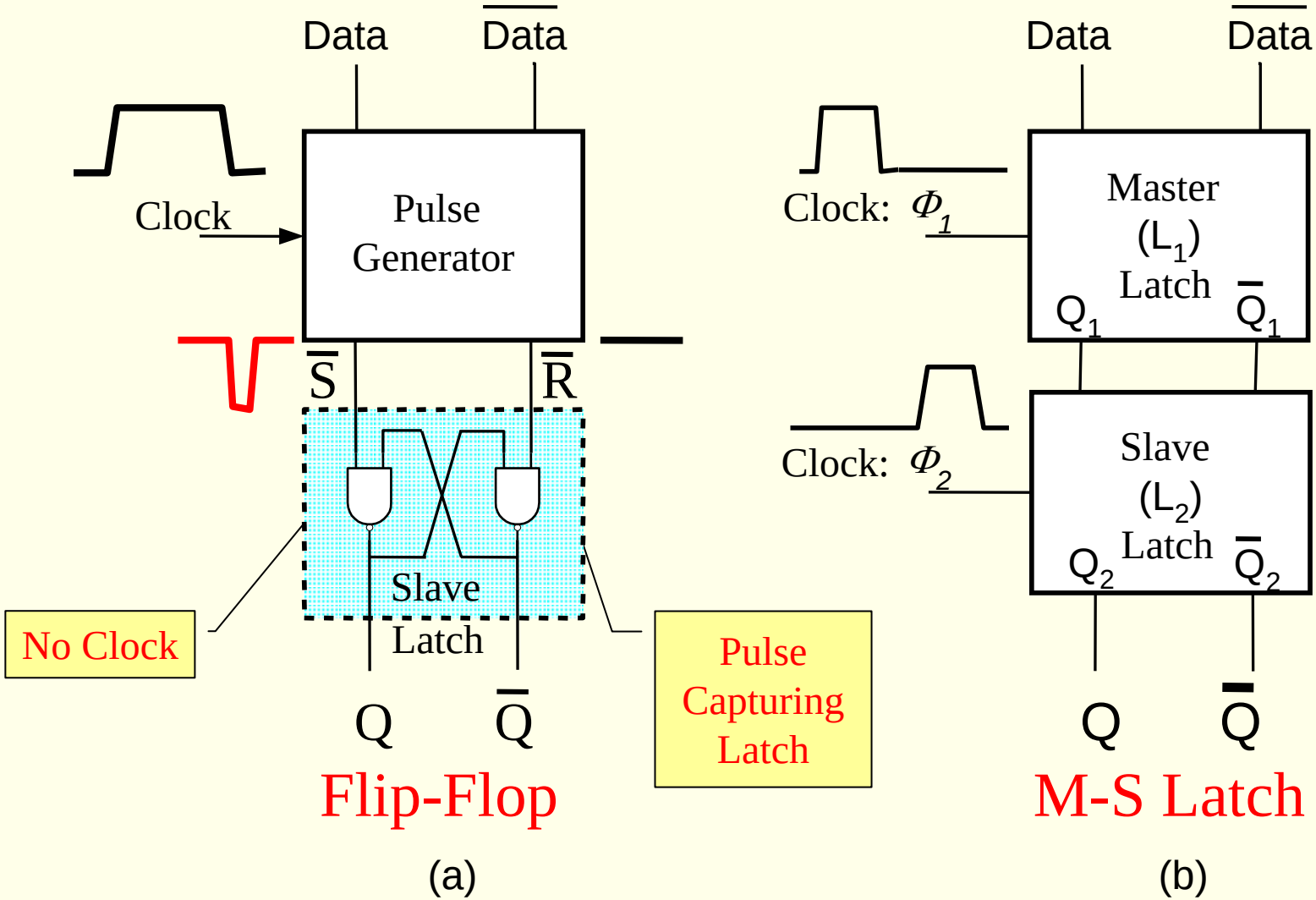


Flip-flop



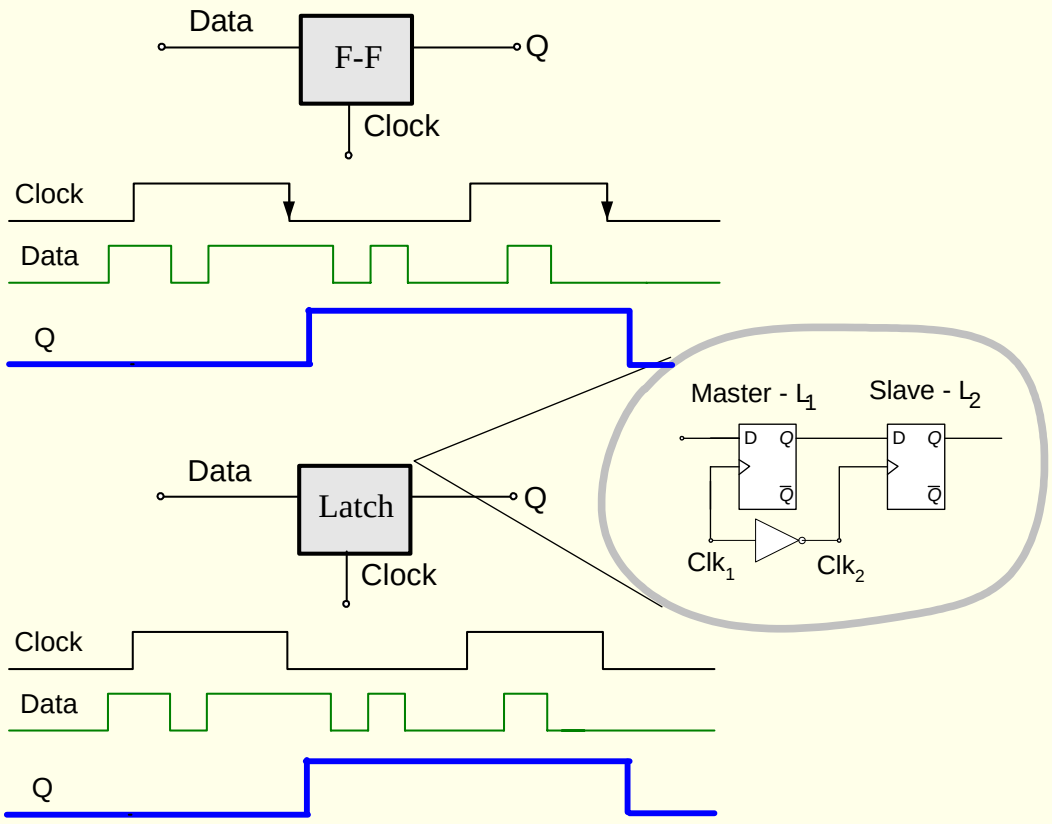
(a) Early version of a flip-flop; (b) PDP-8 direct set-reset sequential element

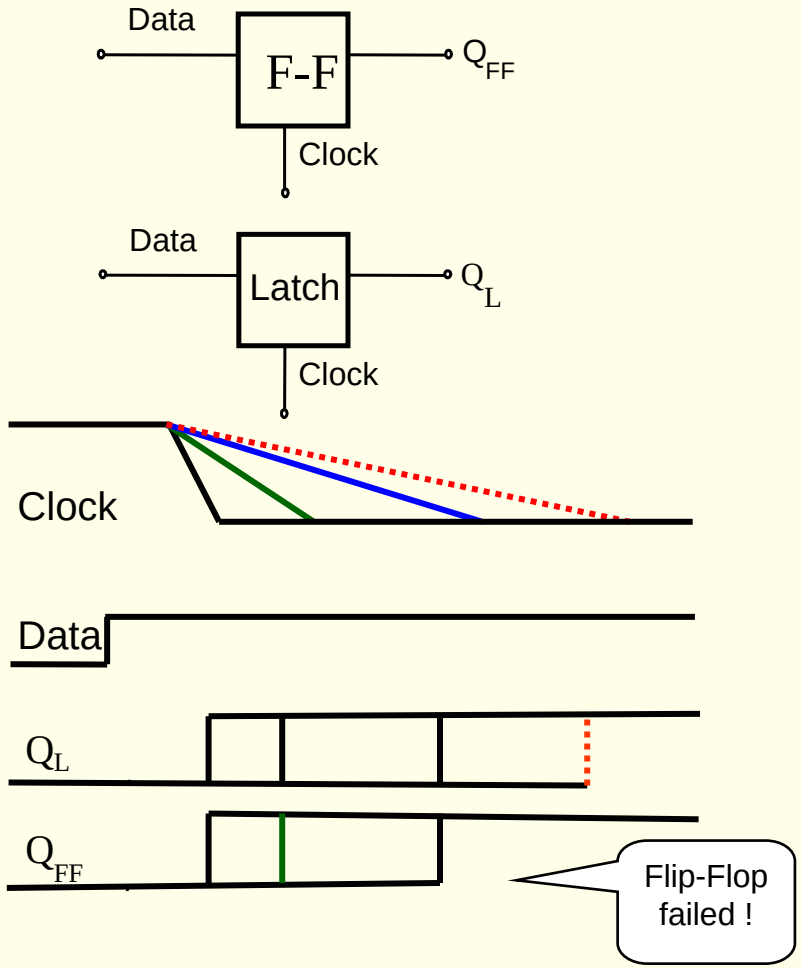
Difference between Flip-flop and M-S Latch



(a) General flip-flop structure; (b) general M-S latch structure

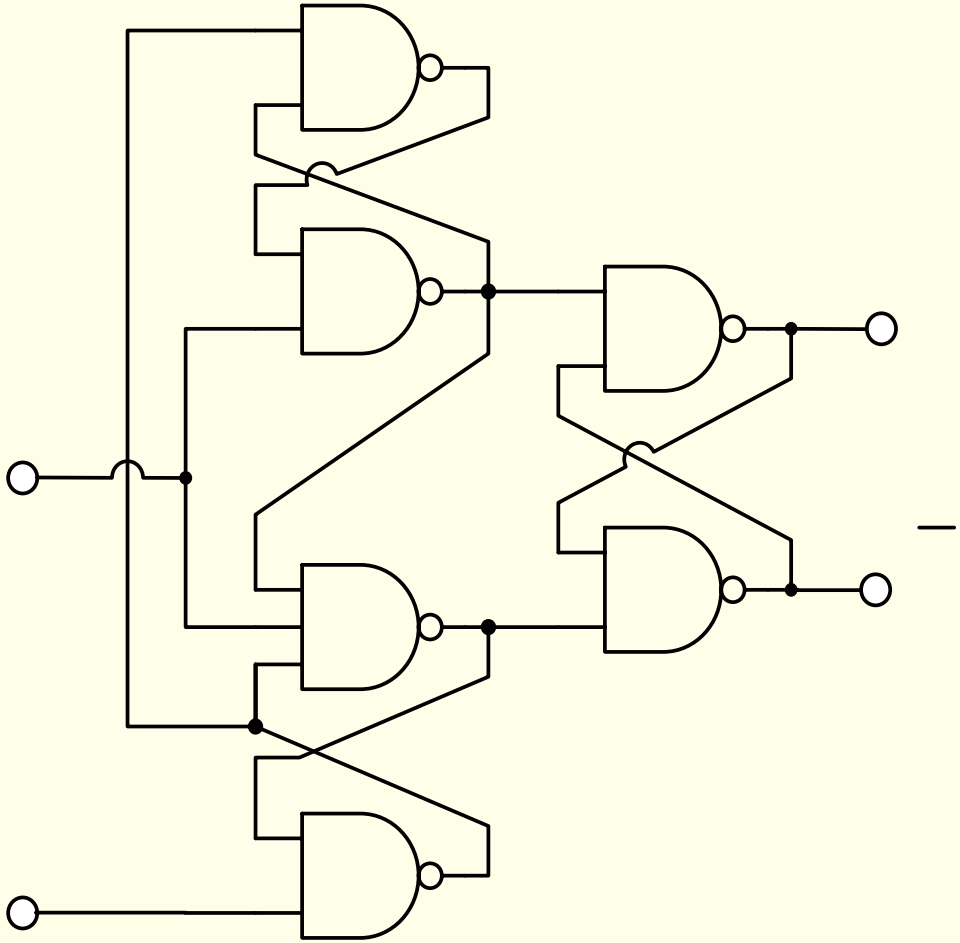
Black-box view of the Flip-flop and M-S latch





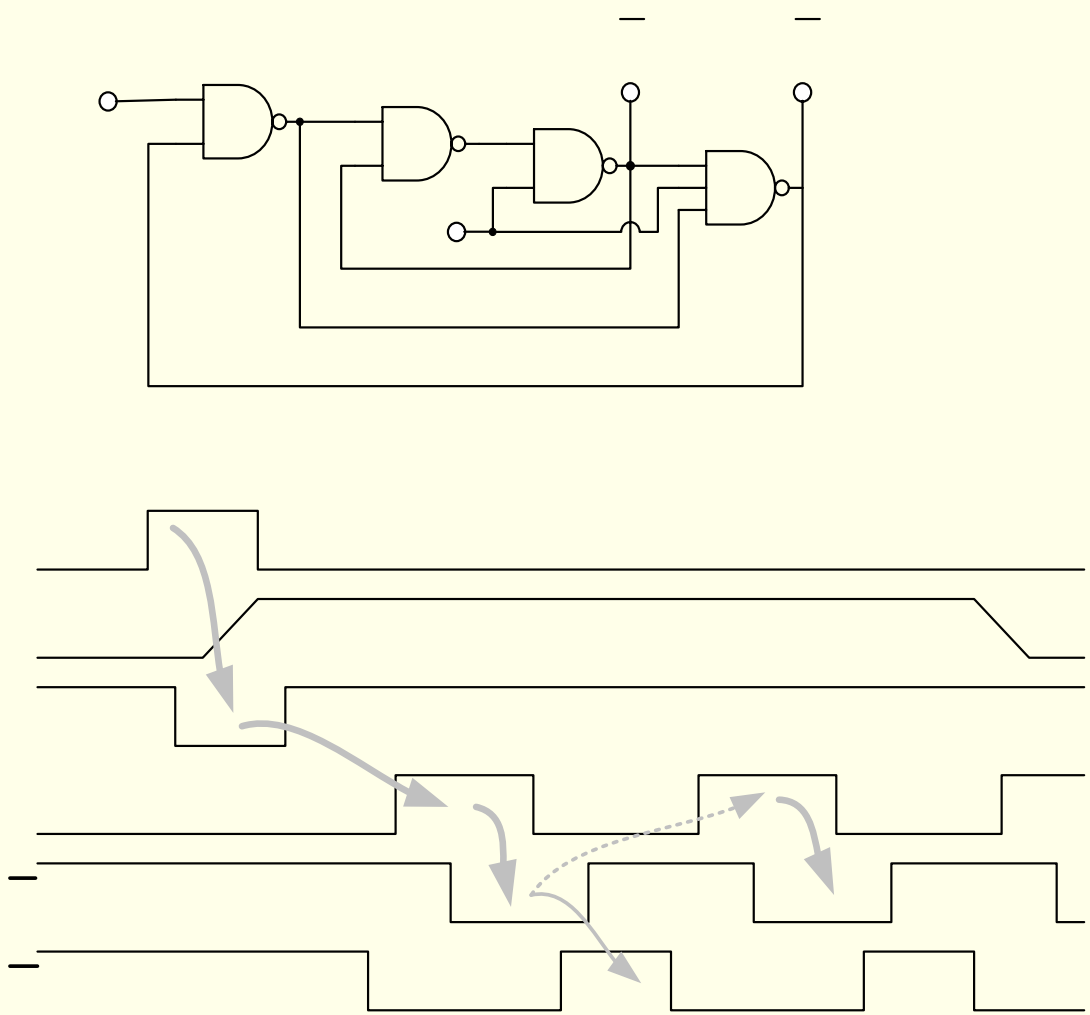
Experiment causing the flip-flop to fail while the M-S latch is still operational

Texas Instruments SN7474 Flip-flop



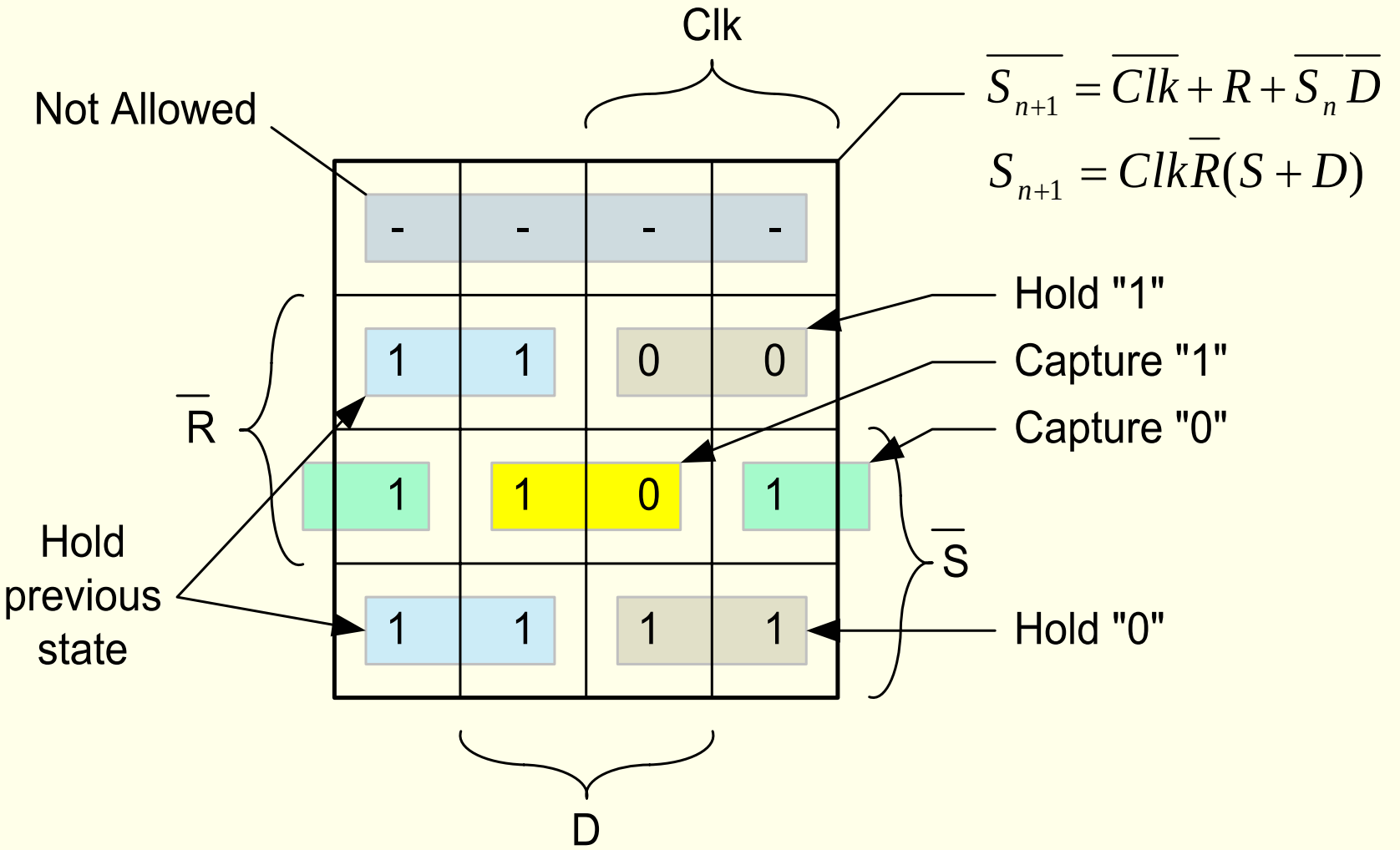
Very much used and analyzed

Pulse generator block of SN7474:
malfunctioning due to a gate-delay

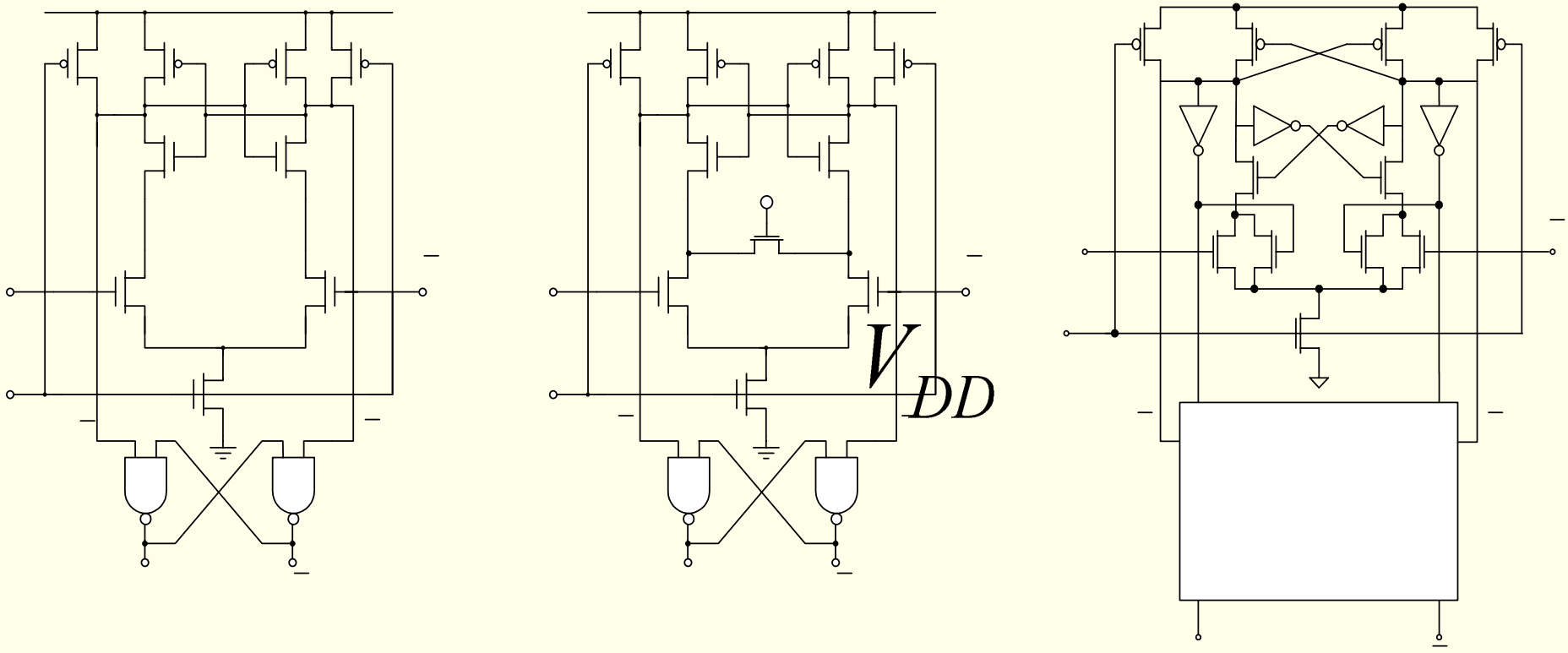


D

Systematic Derivation of a FF using Karnaugh map



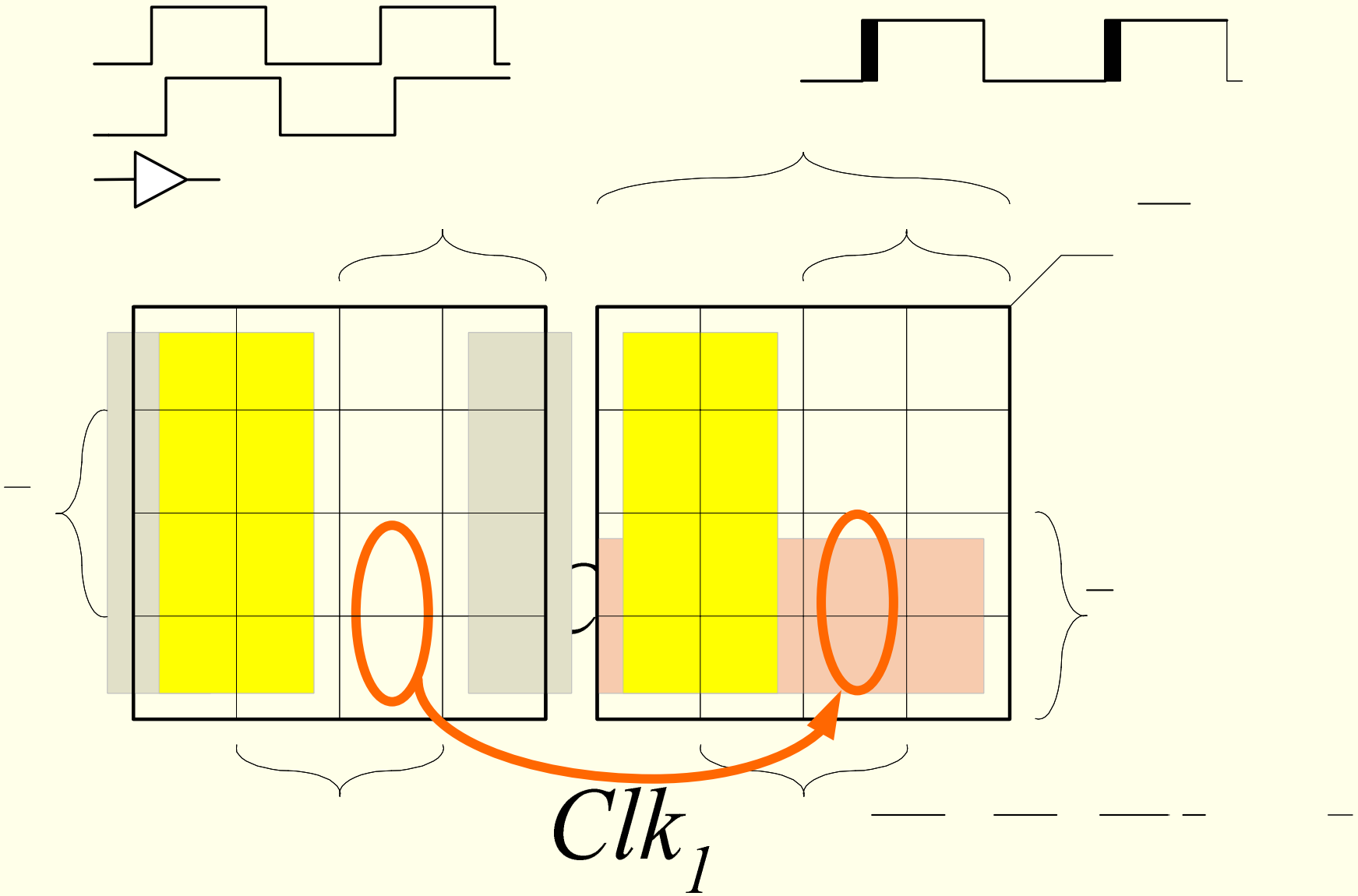
Derivation of the pulse-generating stage of a flip-flop (only the Sn signal is shown)



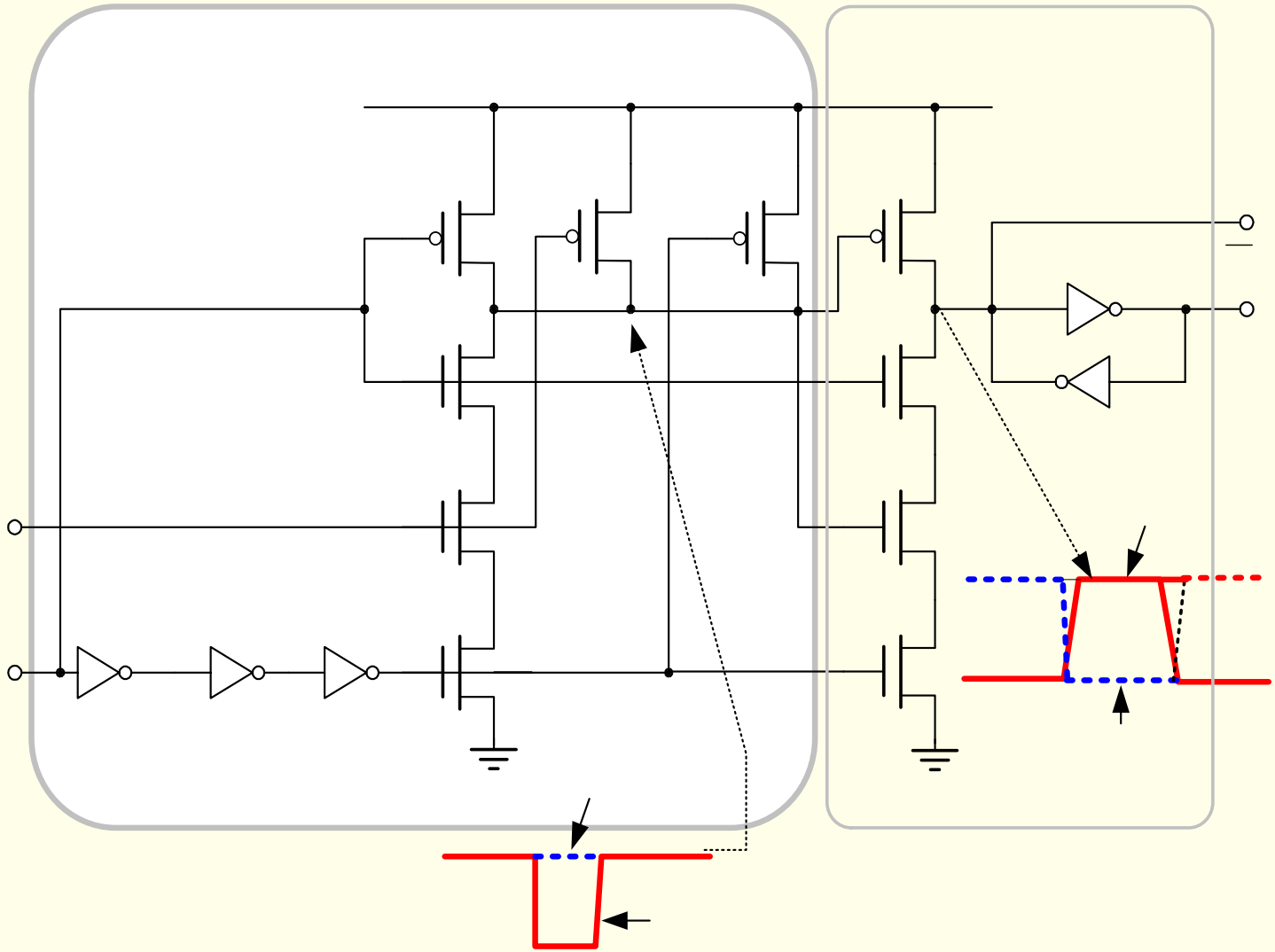
(a) (b) (c)

(a) Pulse generator stage of the sense-amplifier flip-flop. (Madden and Bowhill, 1990);
(b) Improvement for floating nodes. (Dobberpuhl, 1997);
(c) Pulse generator stage improvement by proper design. (Nikolic and Oklobdzija, 1999).

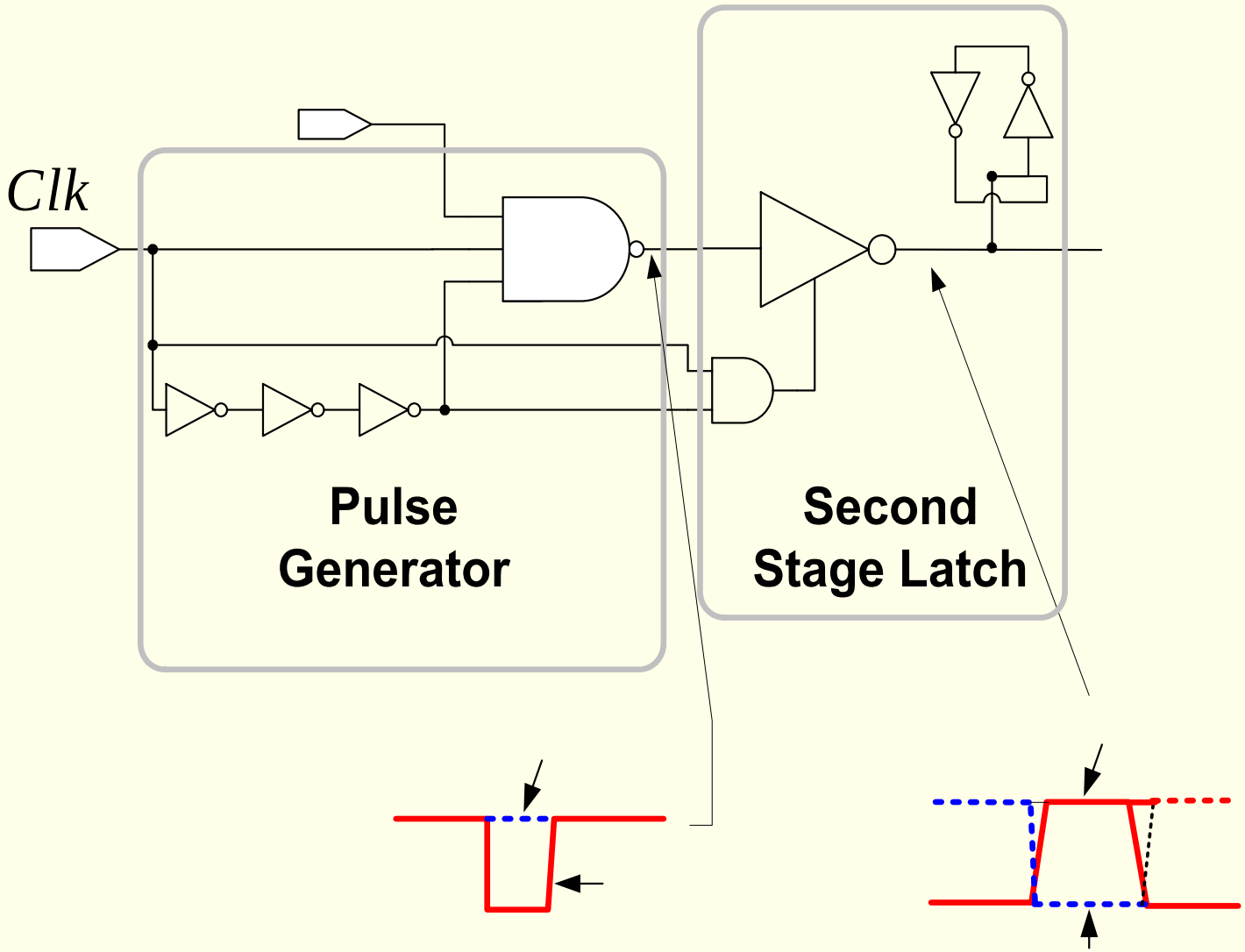
Creating the time reference points for opening and shutting the flip-flop



Hybrid-Latch Flip-Flop (HLFF) introduced by Partovi at al.

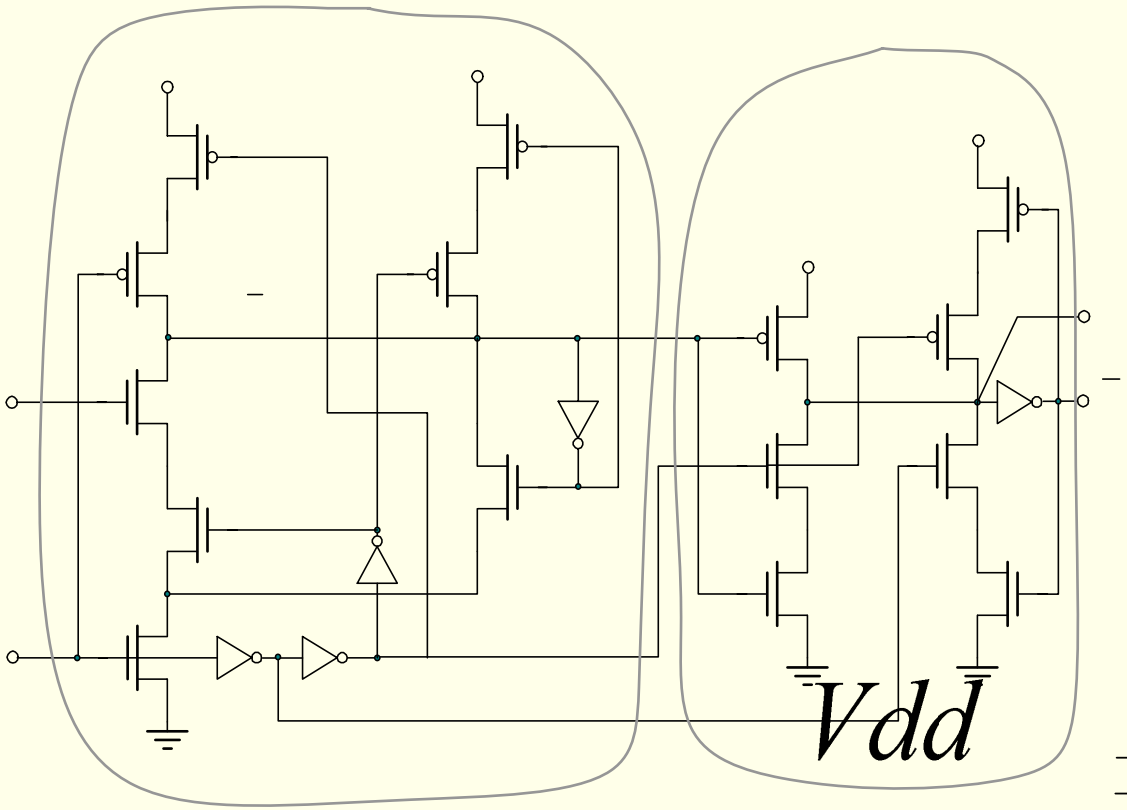


Logic representation of Partovi's flip-flop (HLFF)

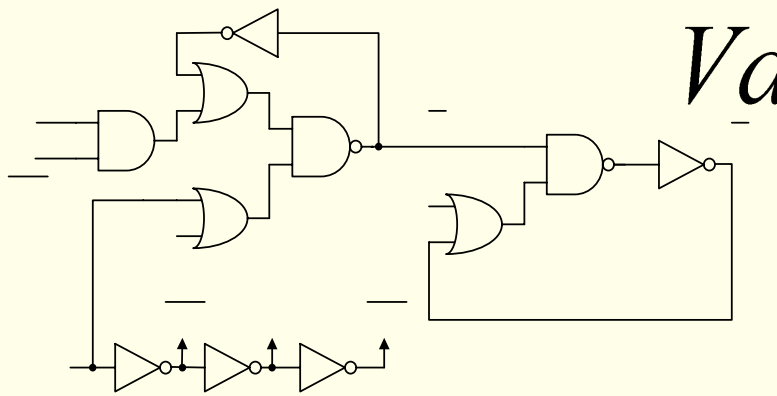


Systematically derived single-ended flip-flop

(according to the slide no. 18)



(a)



(b)

(a) circuit diagram; (b) logic representation.

(Nedovic and Oklobdzija, 2000). Copyright © 2000 IEEE

M_{P1} M_{P3}