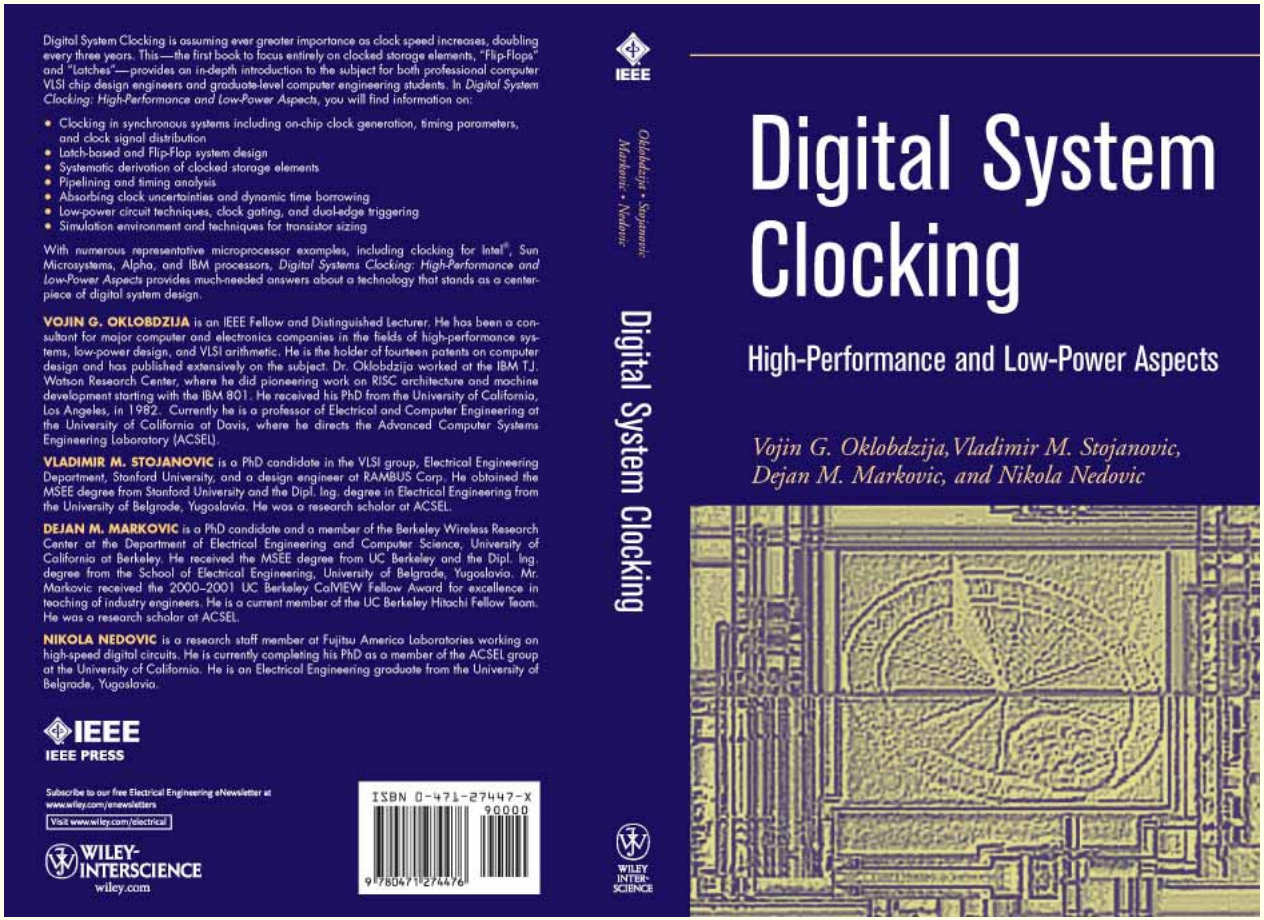
Digital System Clocking:

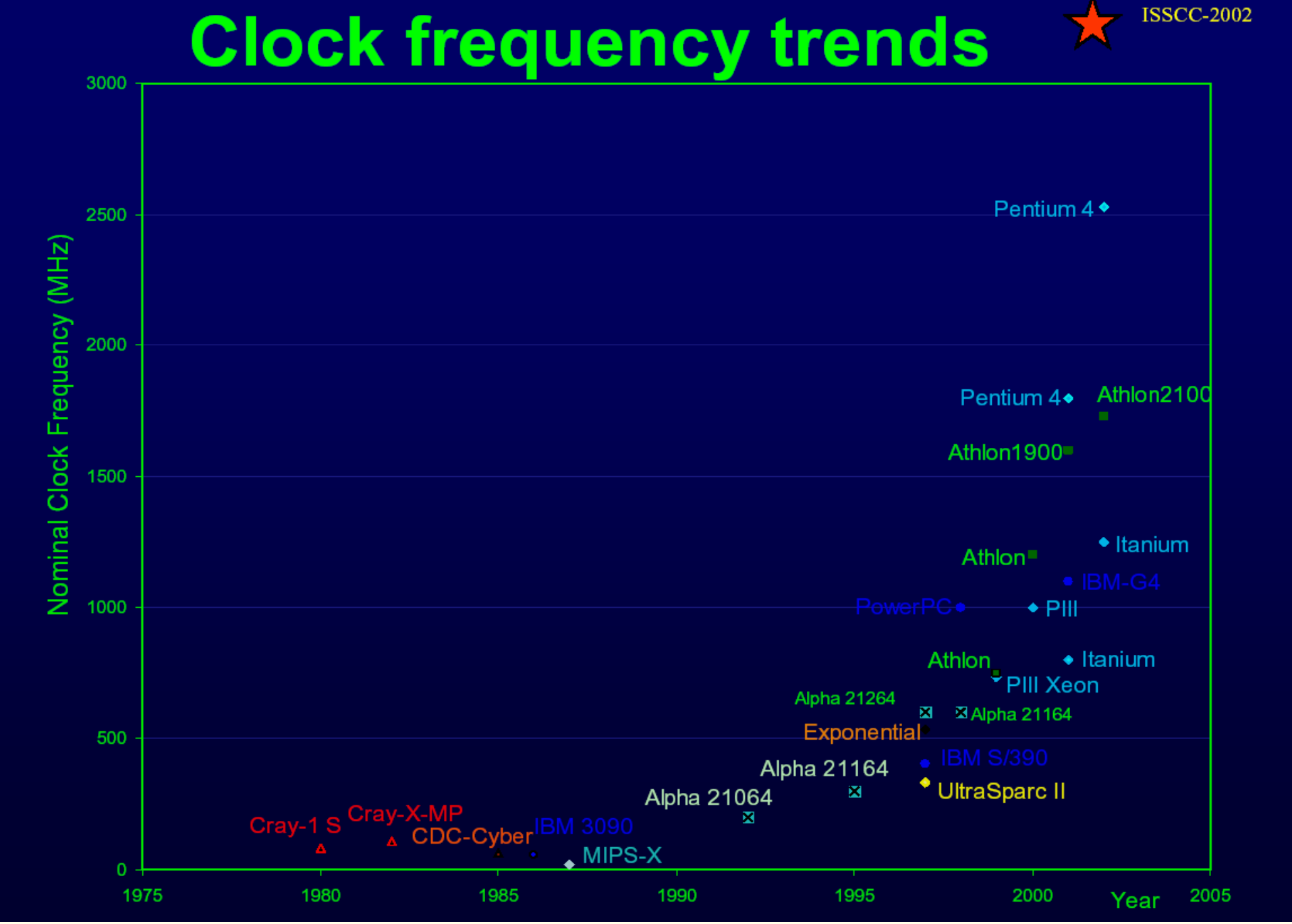
High-Performance and Low-Power Aspects

Vojin G. Oklobdzija, Vladimir M. Stojanovic, Dejan M. Markovic, Nikola M. Nedovic



Wiley-Interscience and IEEE Press, January 2003

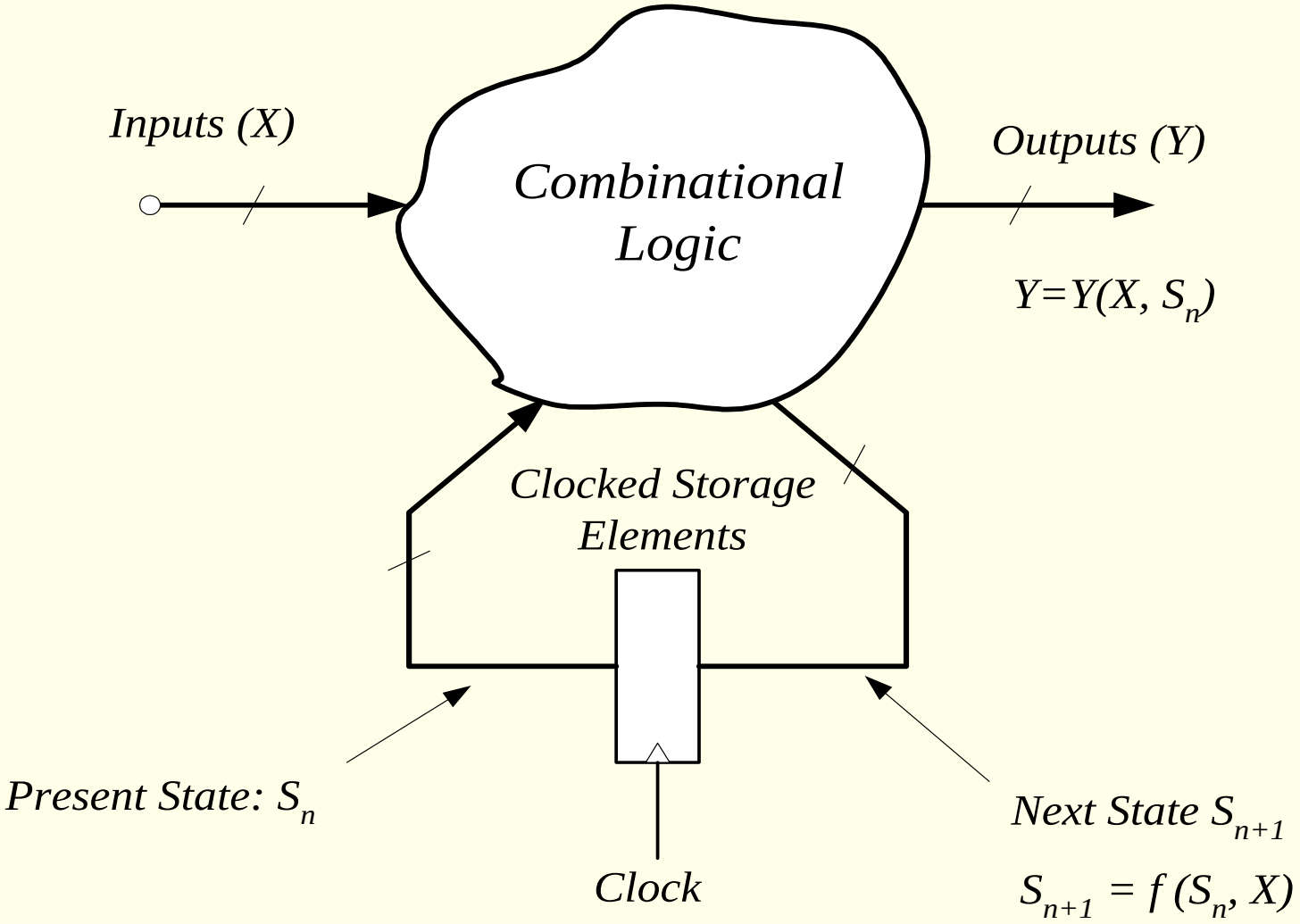
Clock frequency trends



Clock Frequency of Selected Historic Computers and Supercomputers

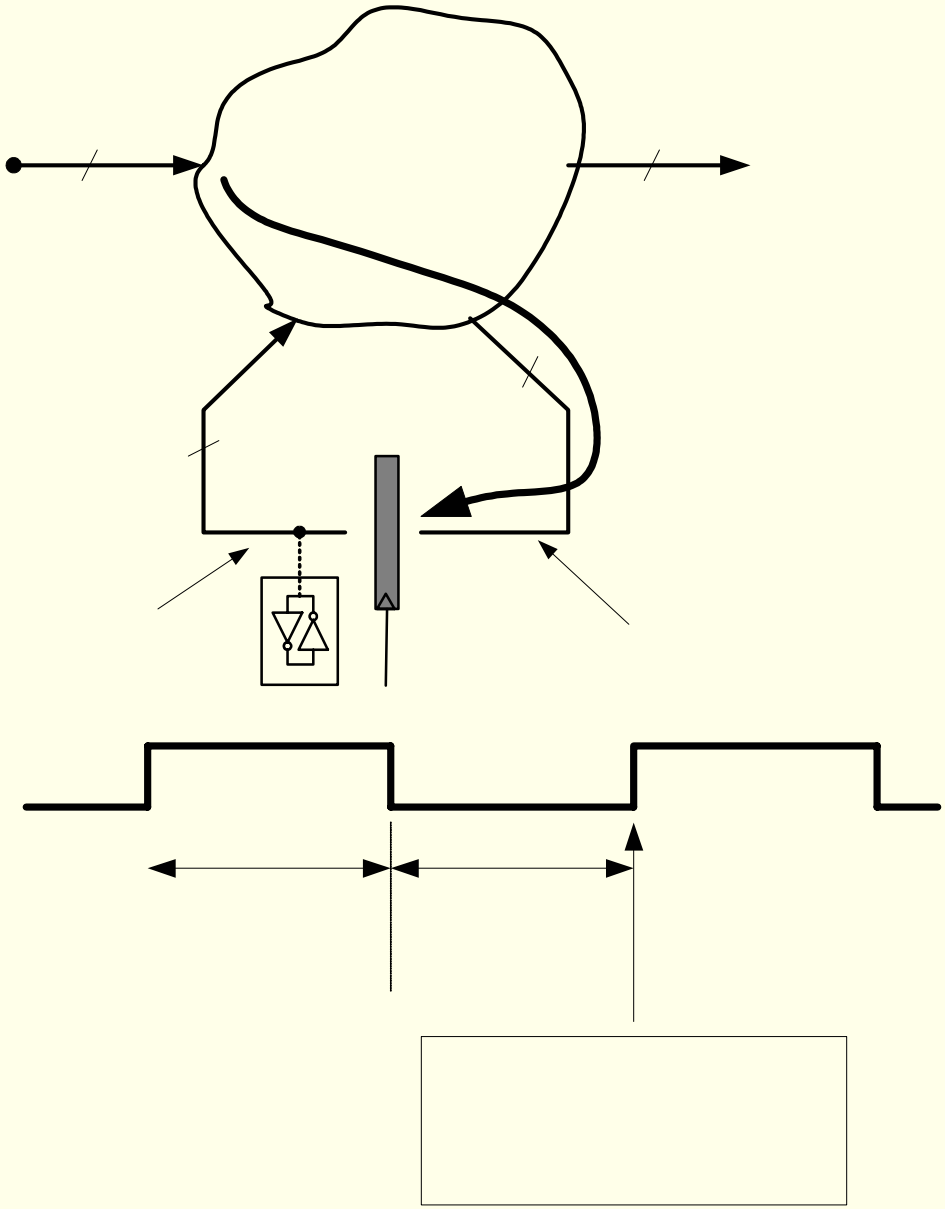
System	Intro Date	Technology	Class	Nominal Clock Period (nS)	Nominal Clock Frequency (MHz)
Cray-X-MP	1982	MSI ECL	Vector Processor	9.5	105.3
Cray-1S,-1M	1980	MSI ECL	Vector Processor	12.5	80.0
CDC Cyber 180/990	1985	ECL	Mainframe	16.0	62.5
IBM 3090	1986	ECL	Mainframe	18.5	54.1
Amdahl 58	1982	LSI ECL	Mainframe	23.0	43.5
IBM 308X	1981	LSI TTL	Mainframe	24.5, 26.0	40.8,38.5
Univac 1100/90	1984	LSI ECL	Mainframe	30.0	33.3
MIPS-X	1987	VLSI CMOS	Microprocessor	50.0	20.0
HP-900	1982	VLSI CMOS	Micro-mainframe	55.6	18.0
Motorola 68020	1985	VLSI CMOS	Microprocessor	60.0	16.7
Bellmac-32A	1982	VLSI CMOS	Microprocessor	125.0	8.0

The concept of Finite-State Machine: FSM (Hoffman Model)



Another Representation of FSM

- Clocked Storage Elements: Flip-Flops and Latches should be viewed as synchronization elements, not merely as storage elements !
- Their main purpose is to synchronize fast and slow paths:
  - prevent the fast path from corrupting the state



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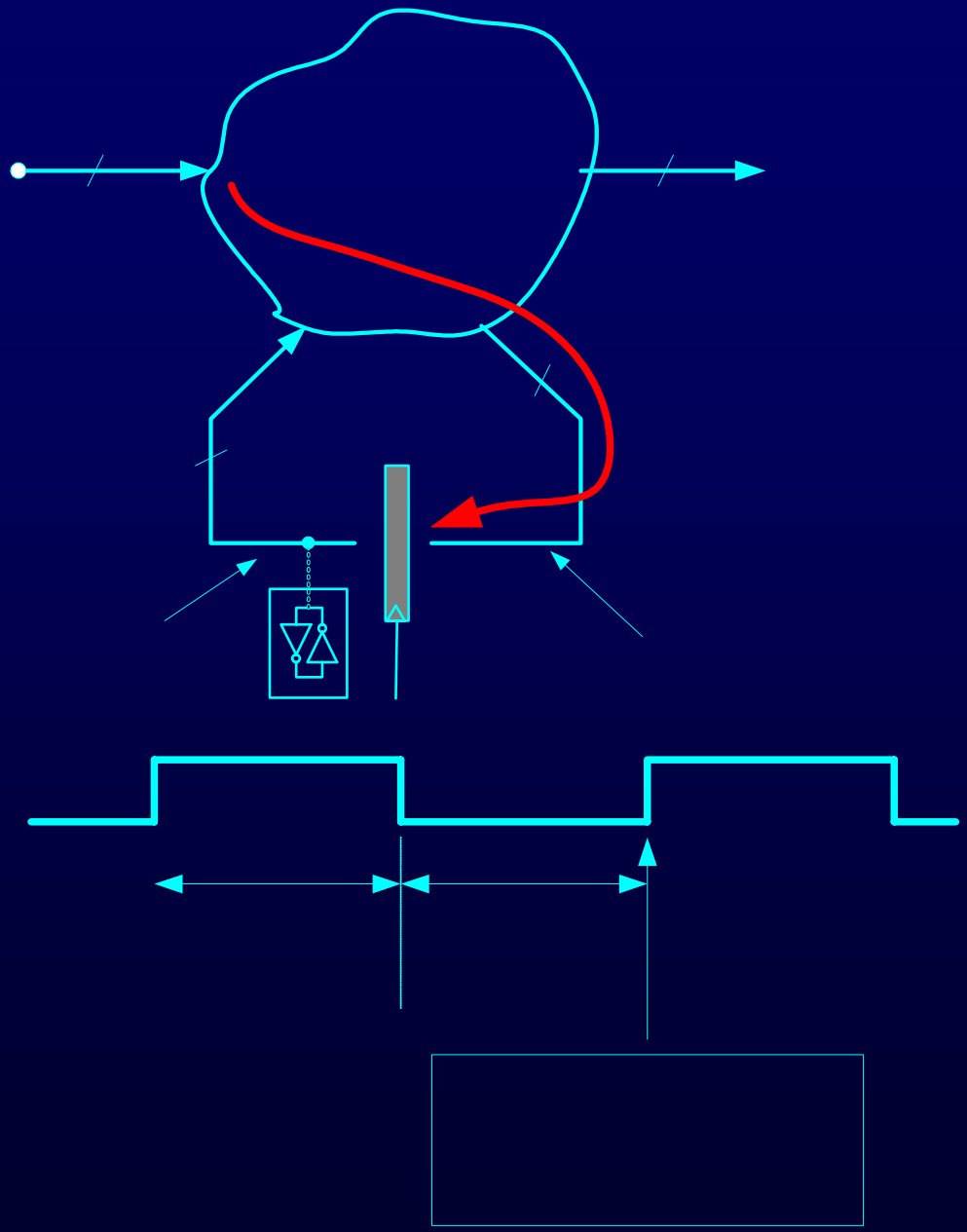


State Changes in the Finite-State Machine

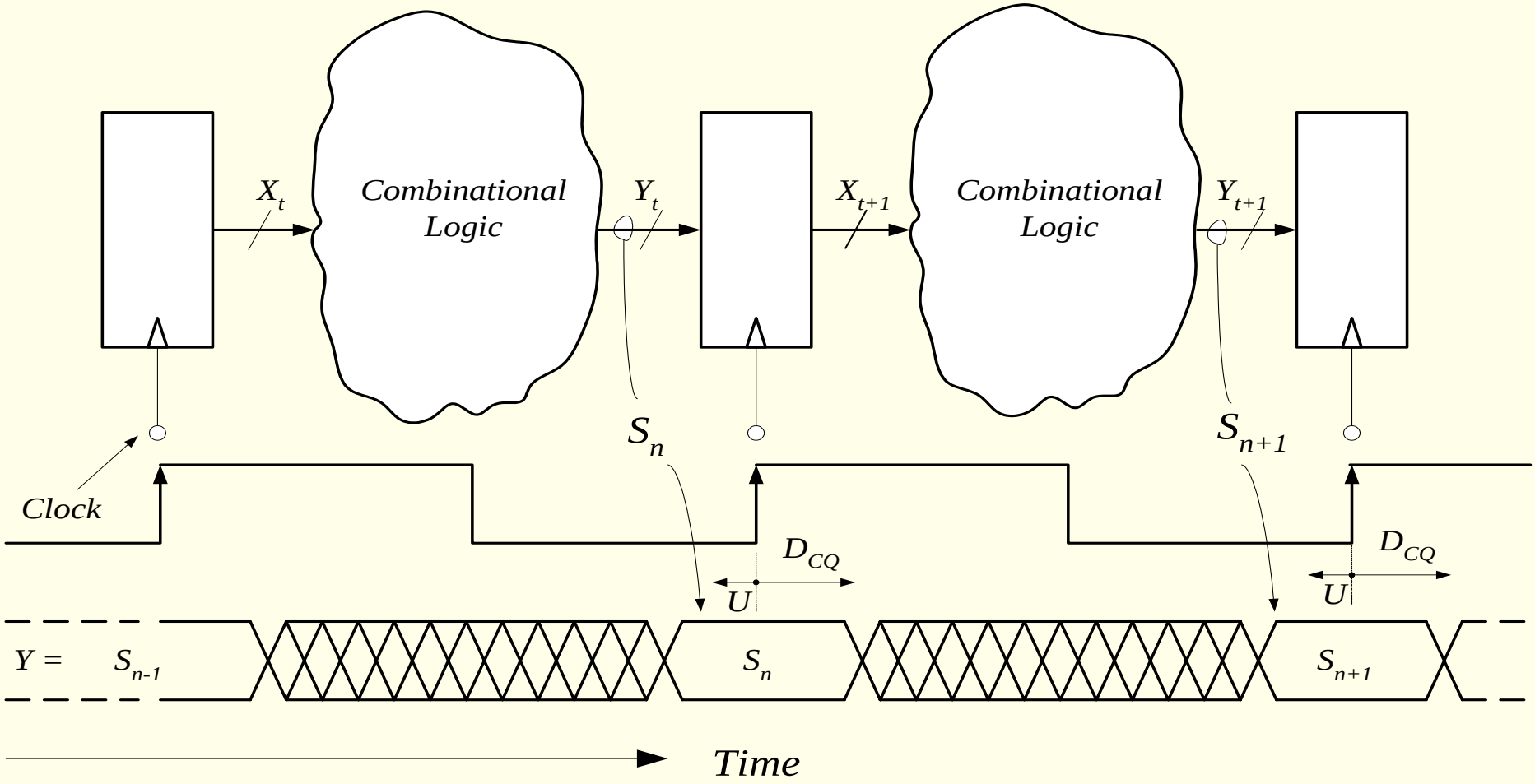
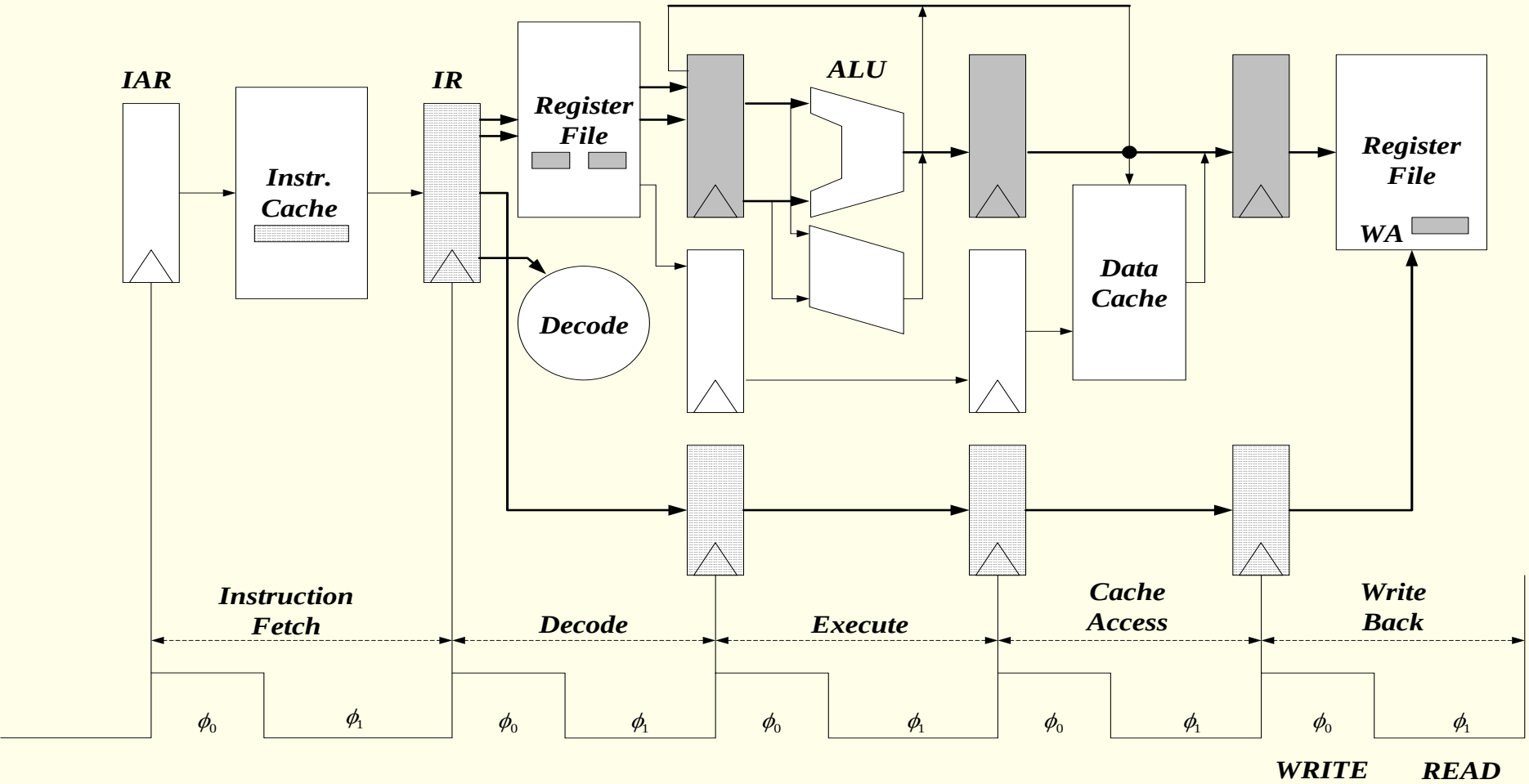
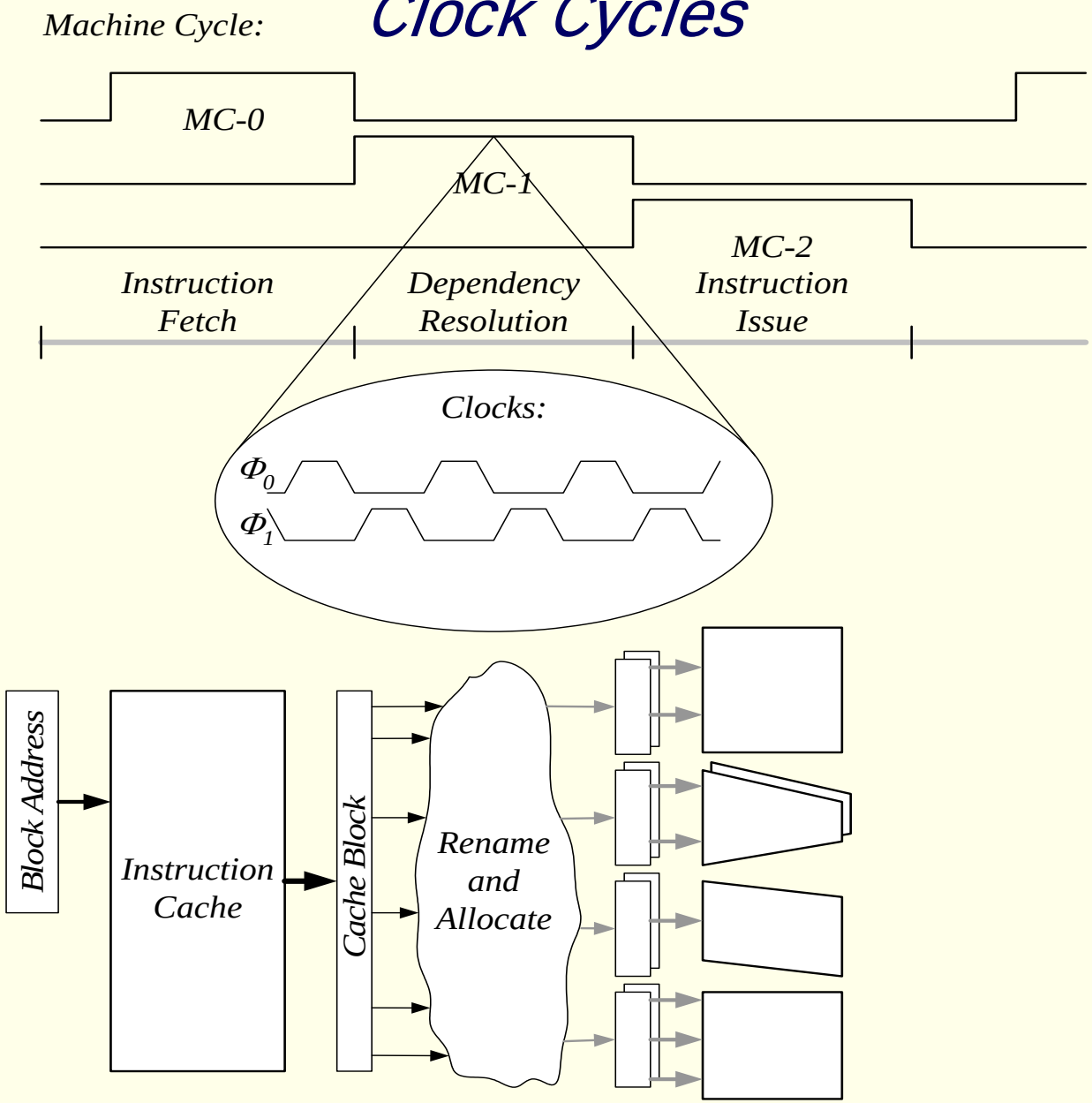


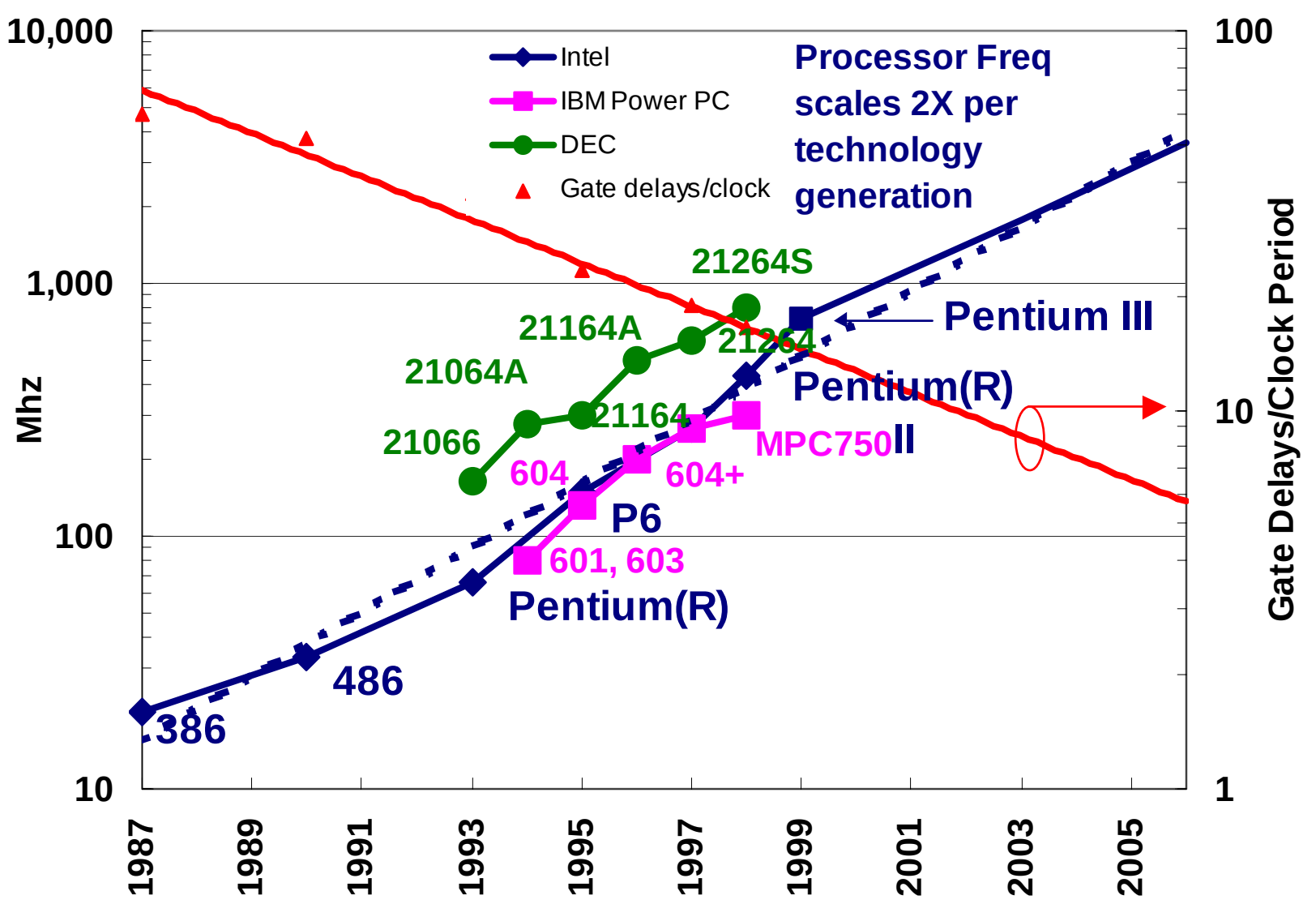
Diagram of a Pipelined System



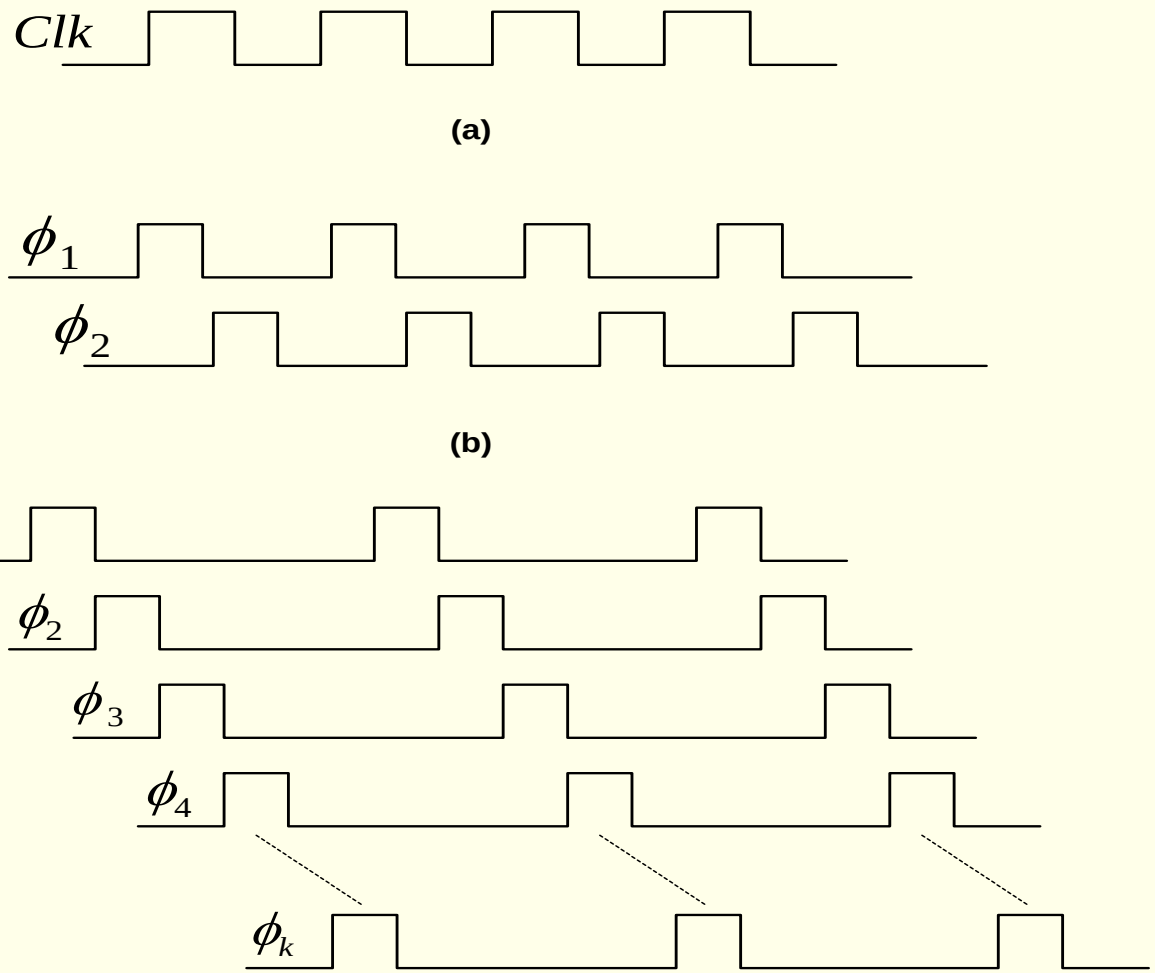
Machine Execution Phases with Respect to the Clock Cycles



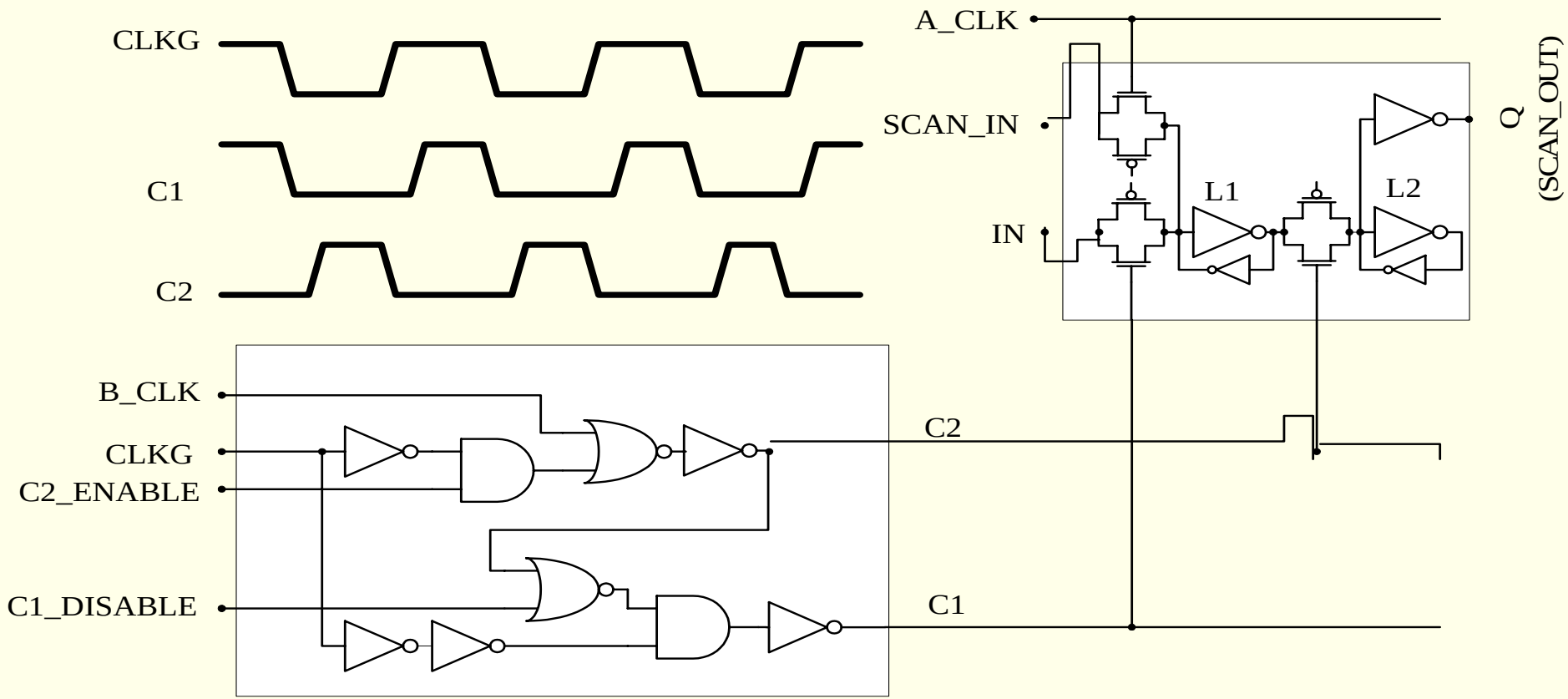
Increase in the Clock Frequency and Decrease in the Number of Logic Levels

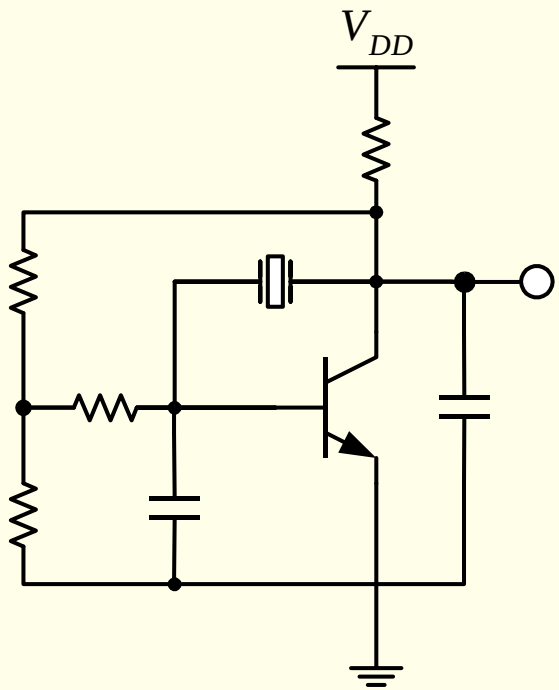


System clocking schemes: *(a) single-phase clock; (b) two-phase clock; (c) multiple-phase clock*

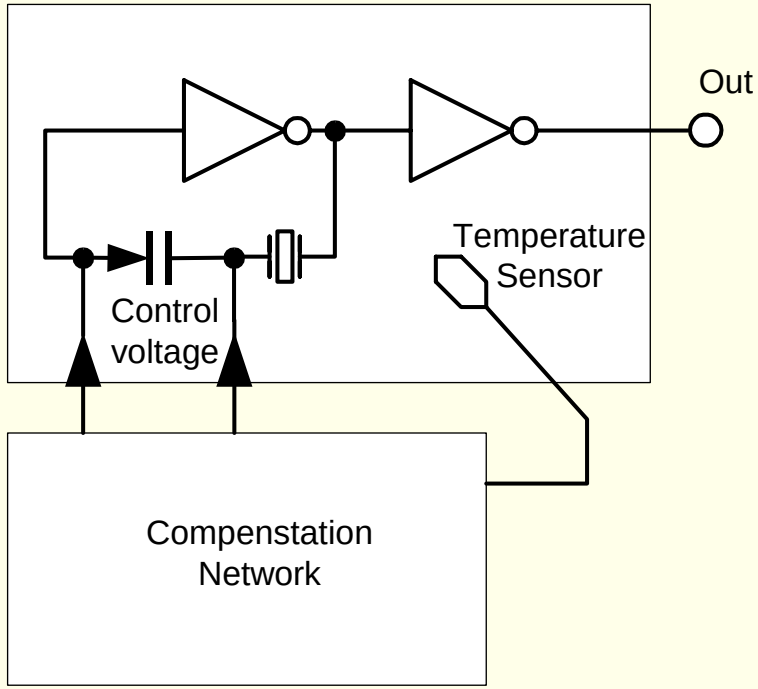


Local generation of Two-Phase Clocks as used in IBM S/390 G4





(a)

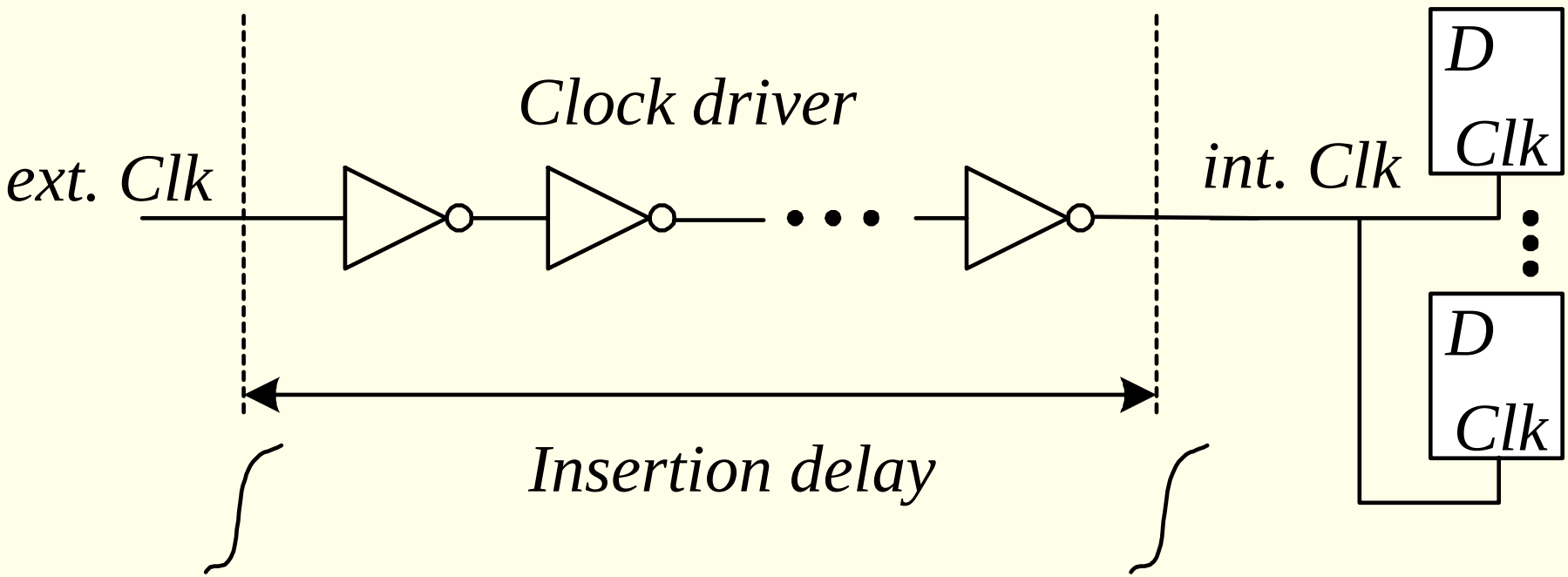


(b)

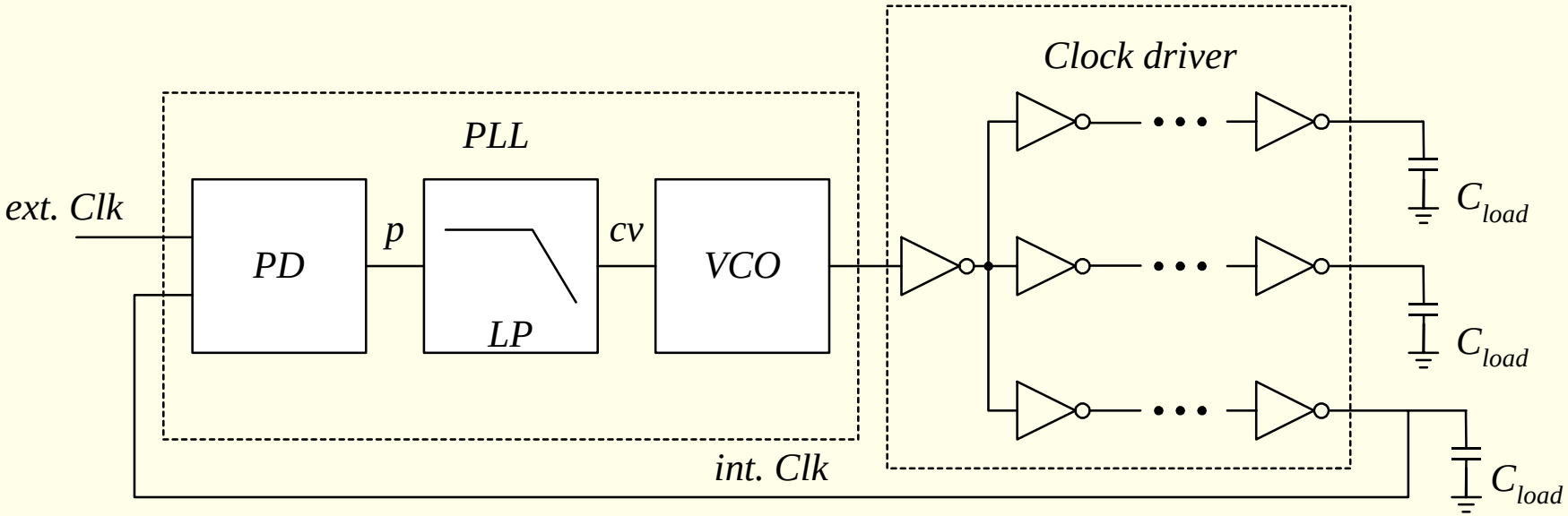
(a) Crystal oscillator

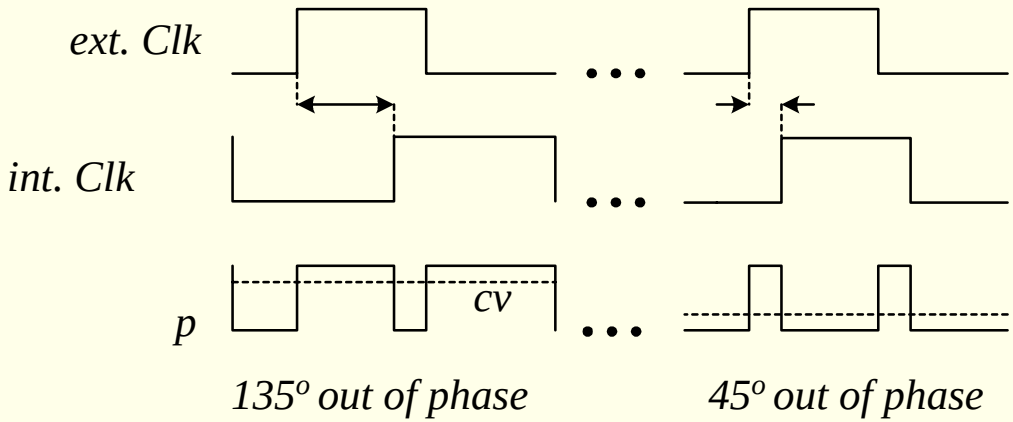
(b) Temperature-compensated crystal oscillator

On-Chip Clock Insertion Delay

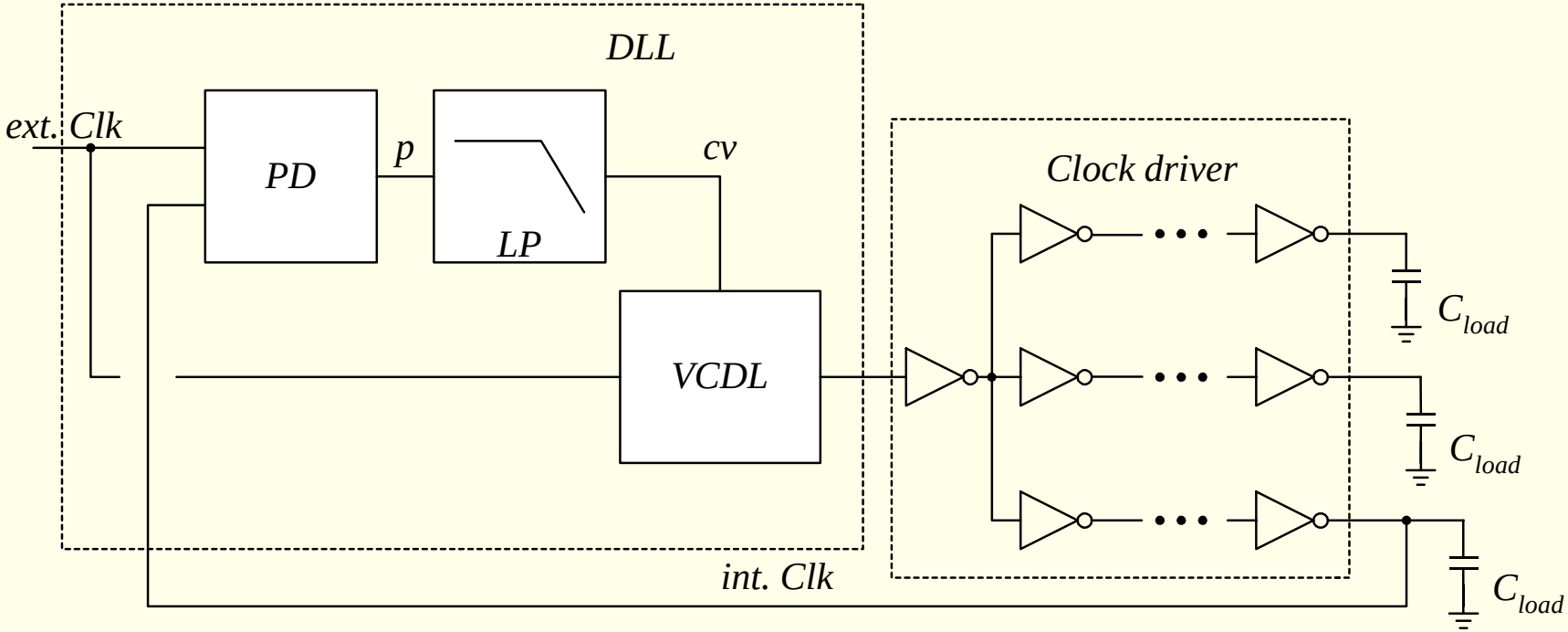


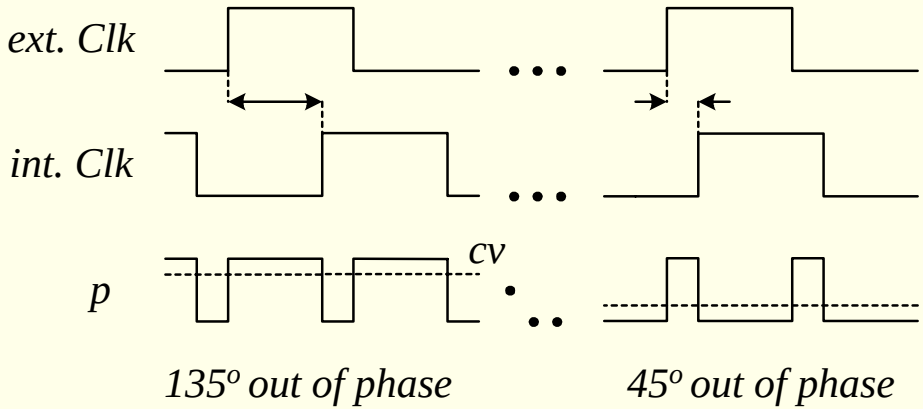
Phase-Locked Loop Block Diagram and Operation



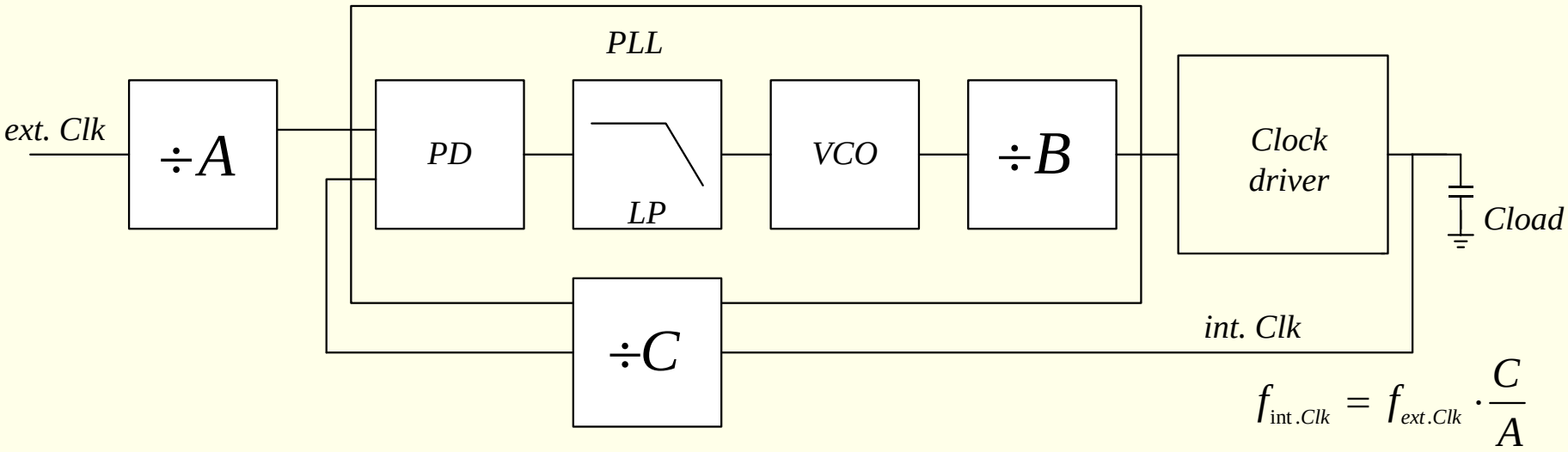


Delay-Locked Loop Block Diagram and Operation

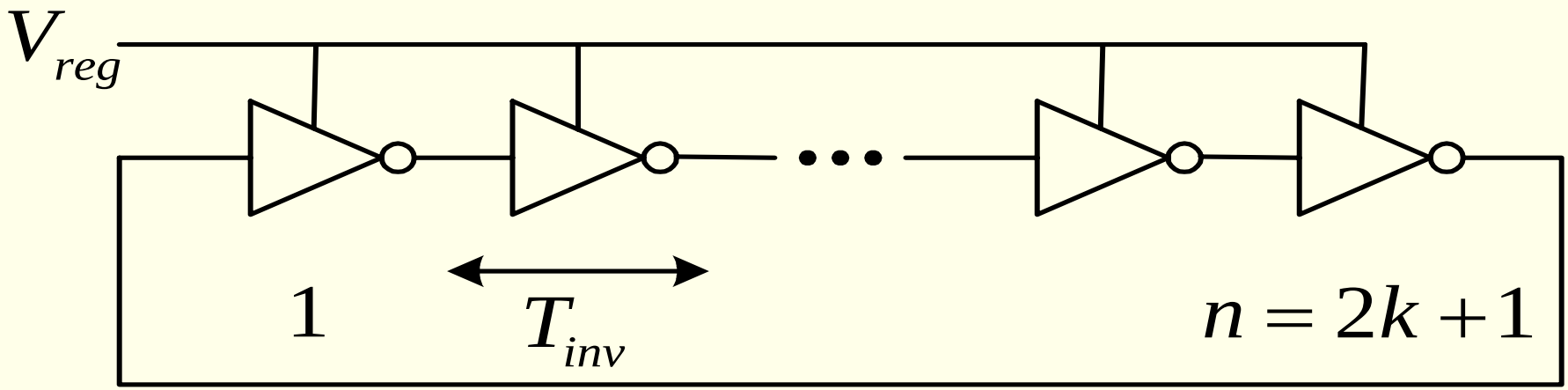




PLL Frequency Multiplication

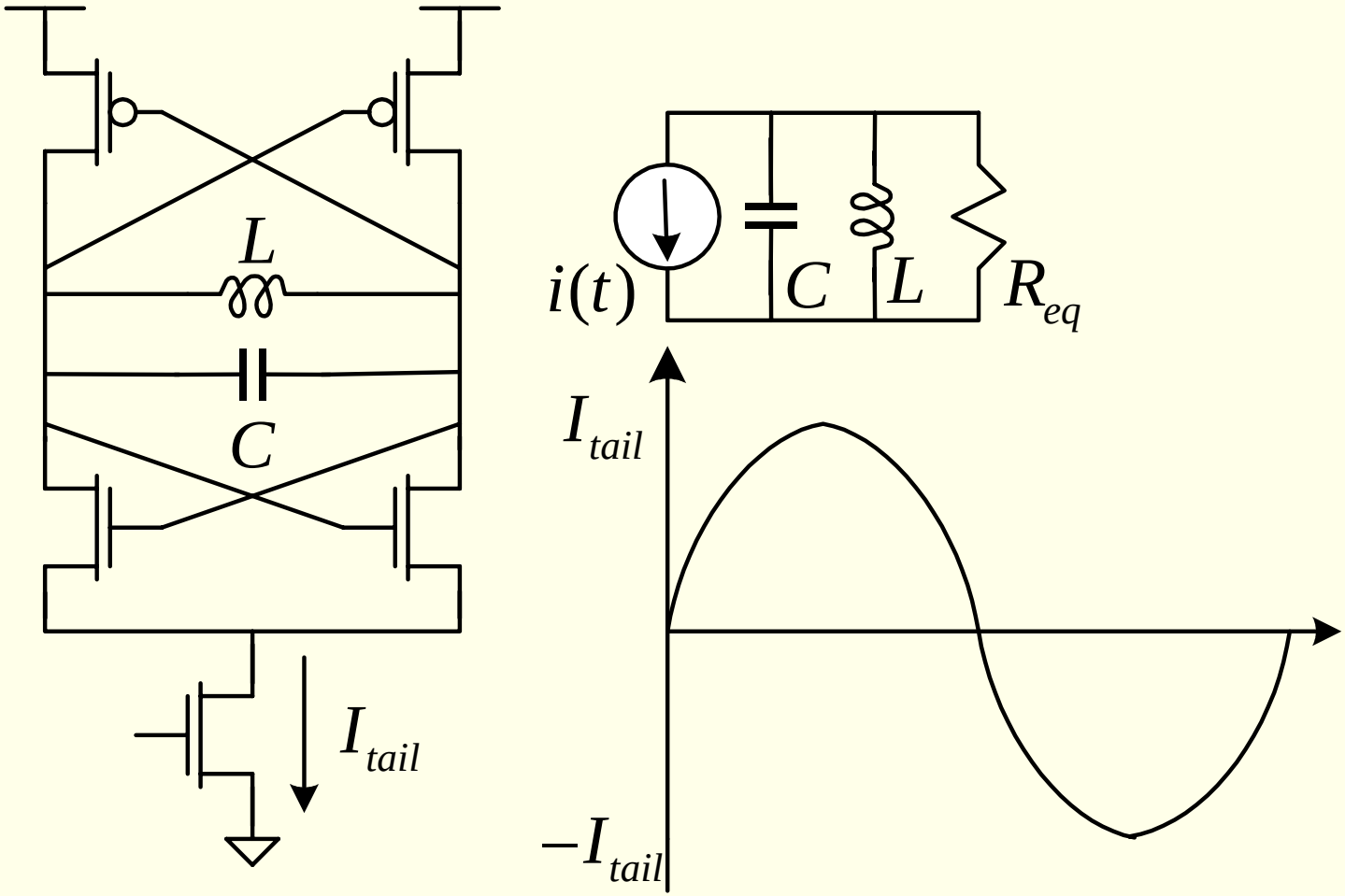


Ring-Oscillator-Based VCO with CMOS Inverters as Delay Elements

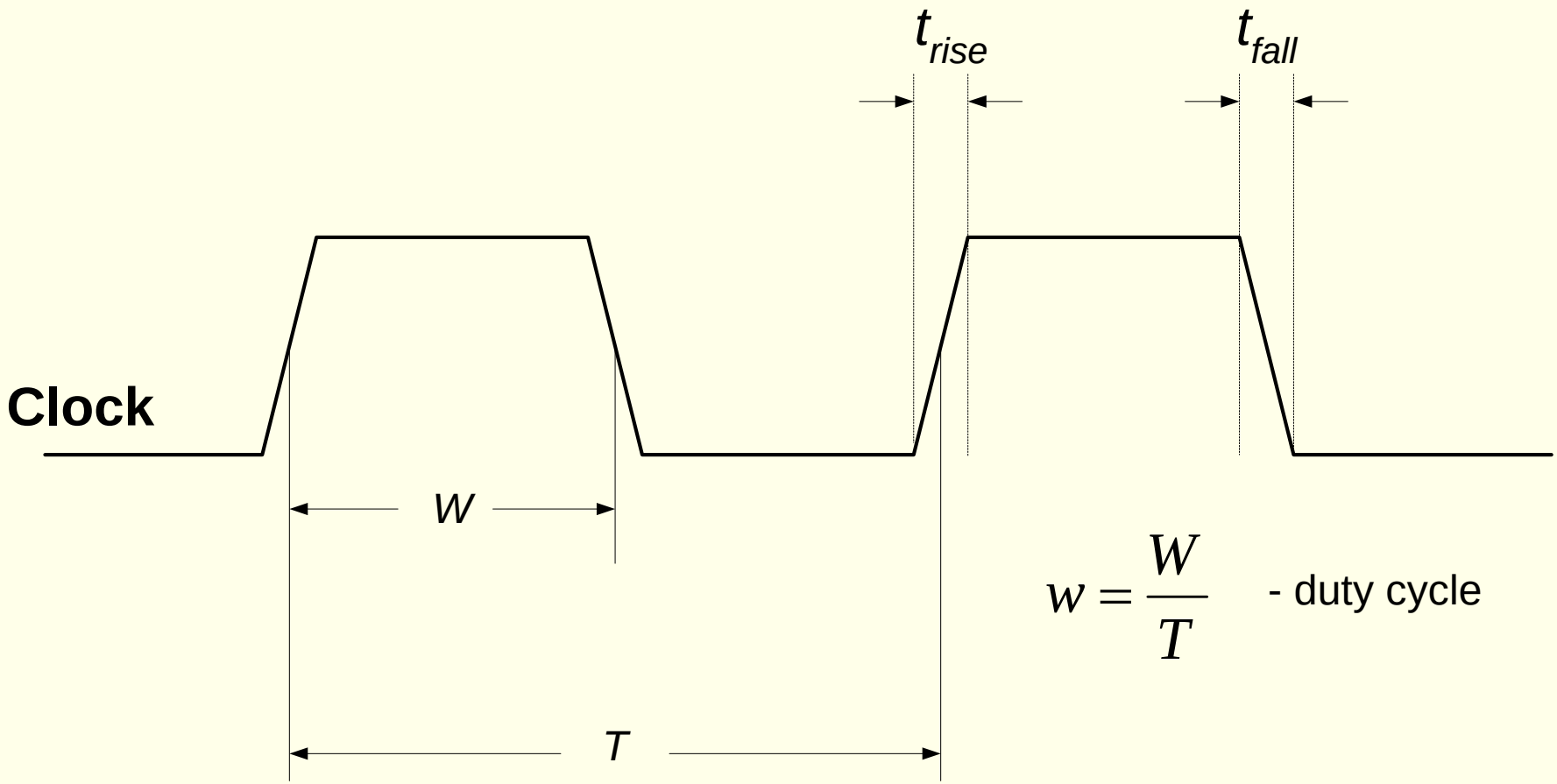


$$f_{osc} = \frac{1}{2nT_{inv}};\ \ k \geq 1$$

LC Tank-Based VCO, Equivalent AC Circuit Model and Current Waveform

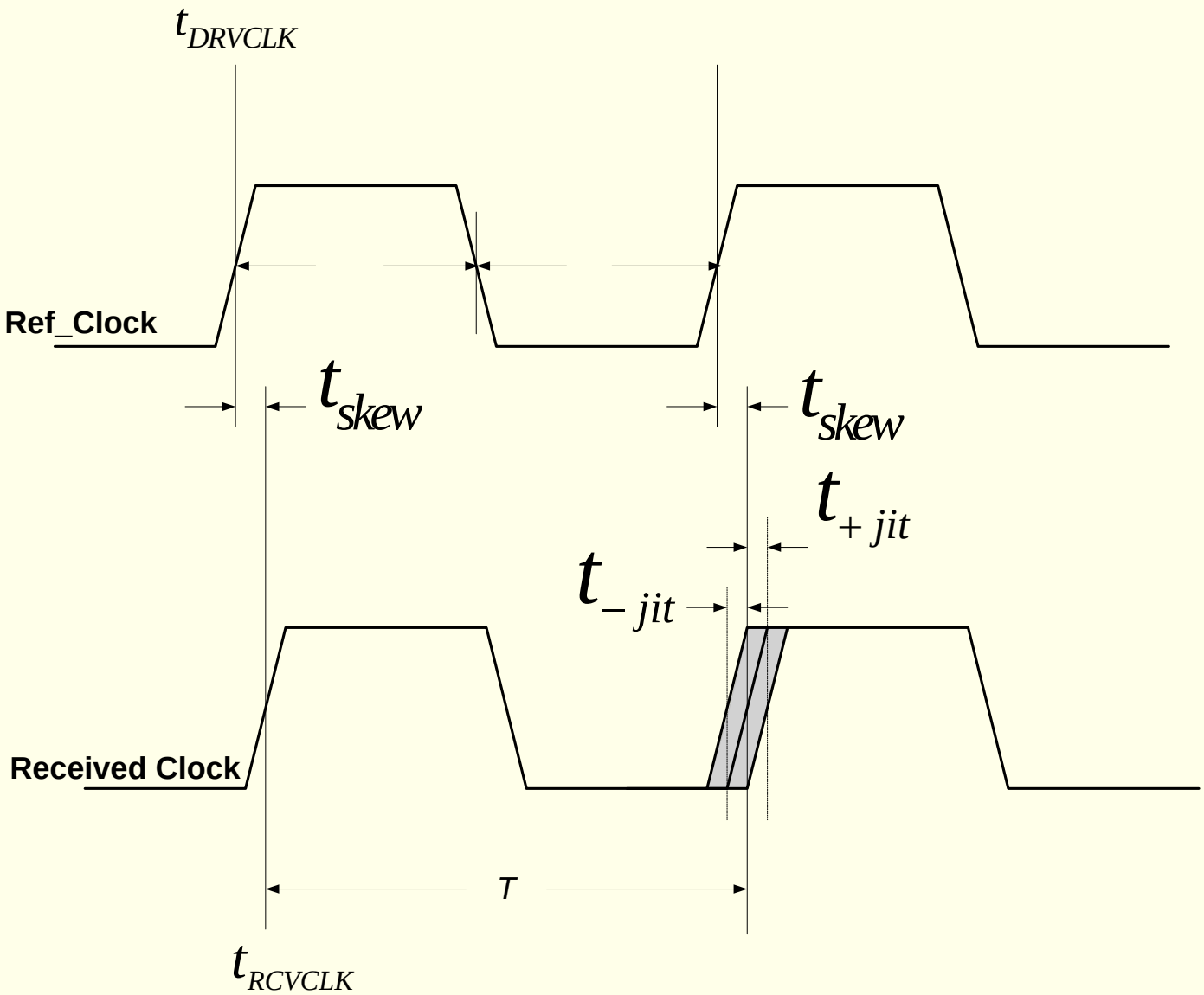


Clock Parameters: Period (T), Width, Rise and Fall Times

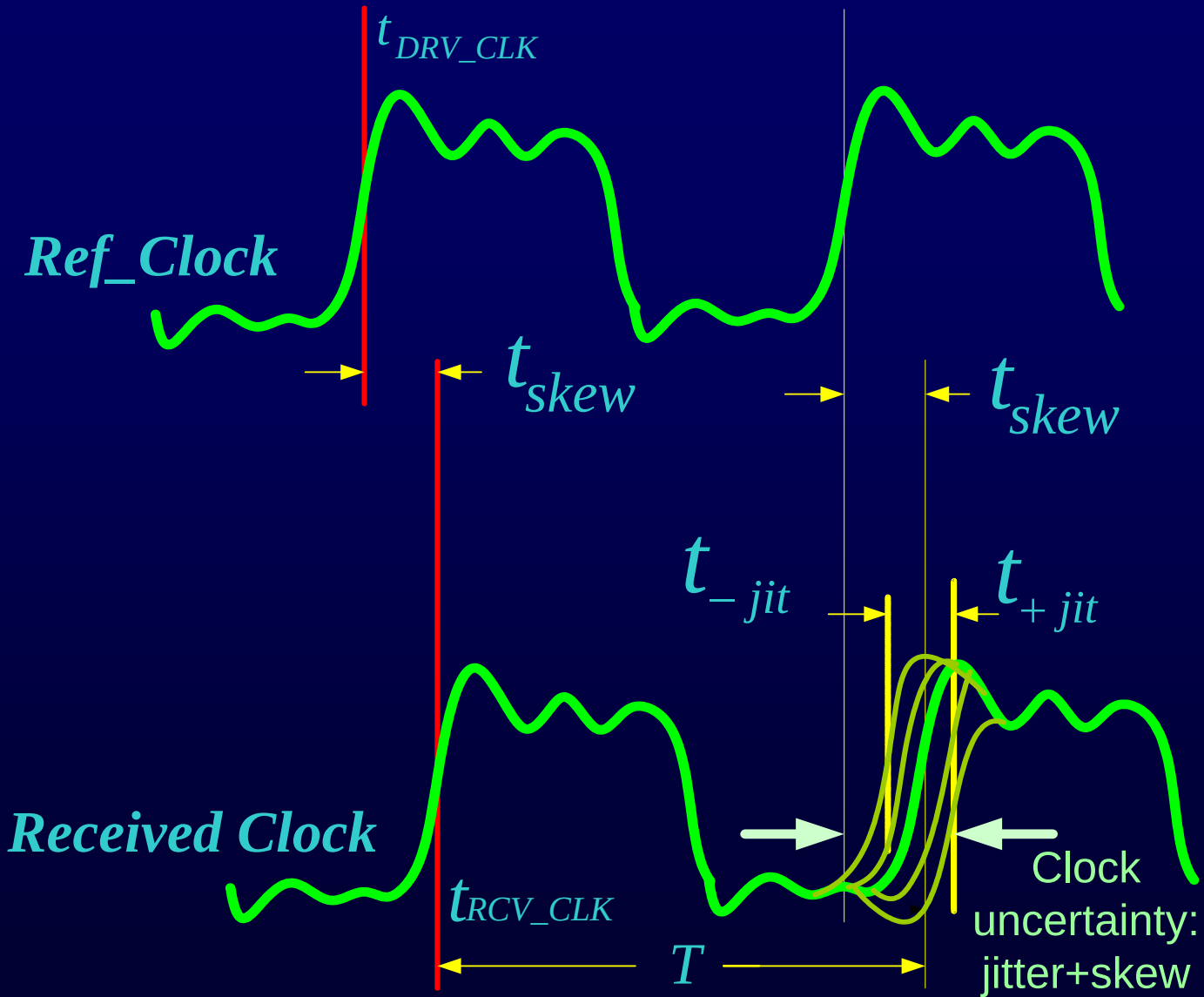


$$w = \frac{W}{T}$$ - duty cycle

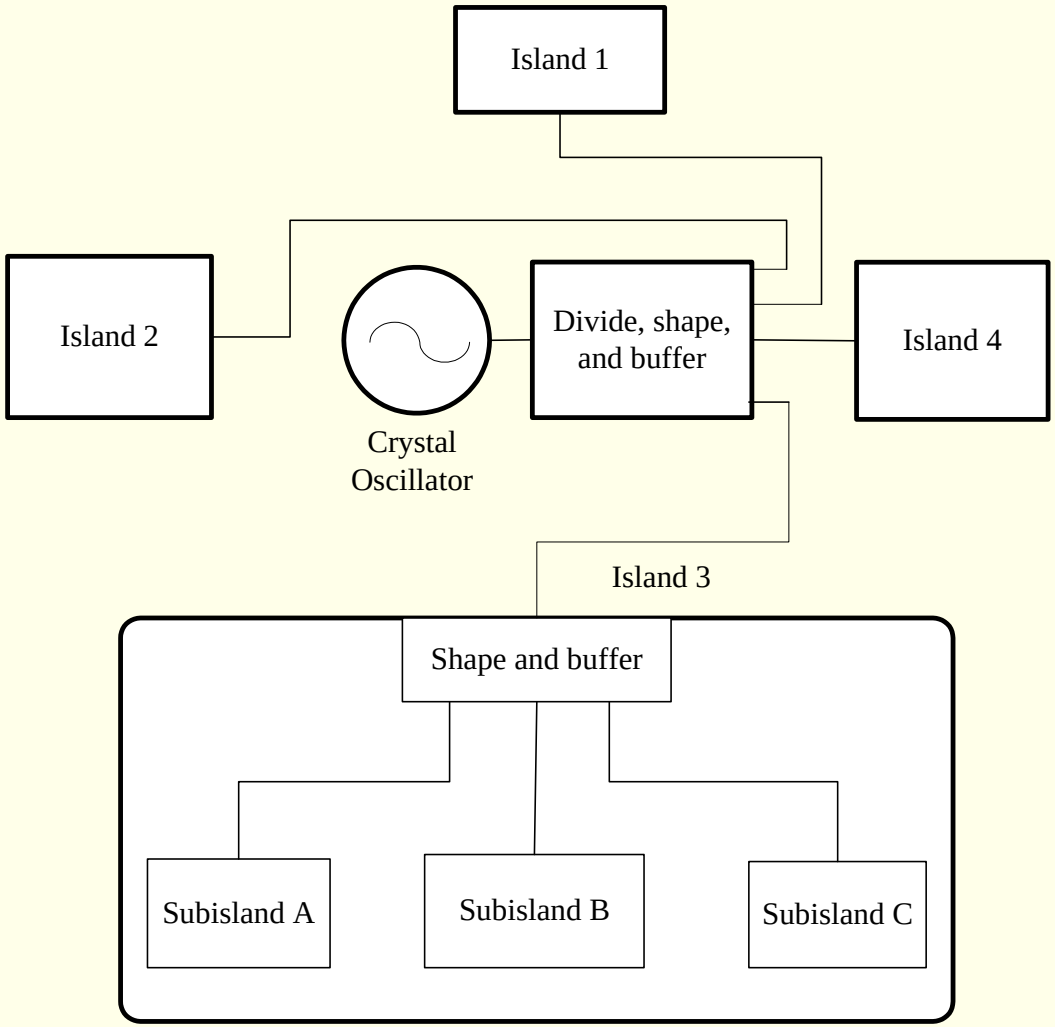
Clock Parameters: Period, Width, Clock Skew and Clock Jitter



Clock Uncertainties



The Concept of Logic Islands (Wagner 1988), Copyright © 1988 IEEE



Clock Tuning Points

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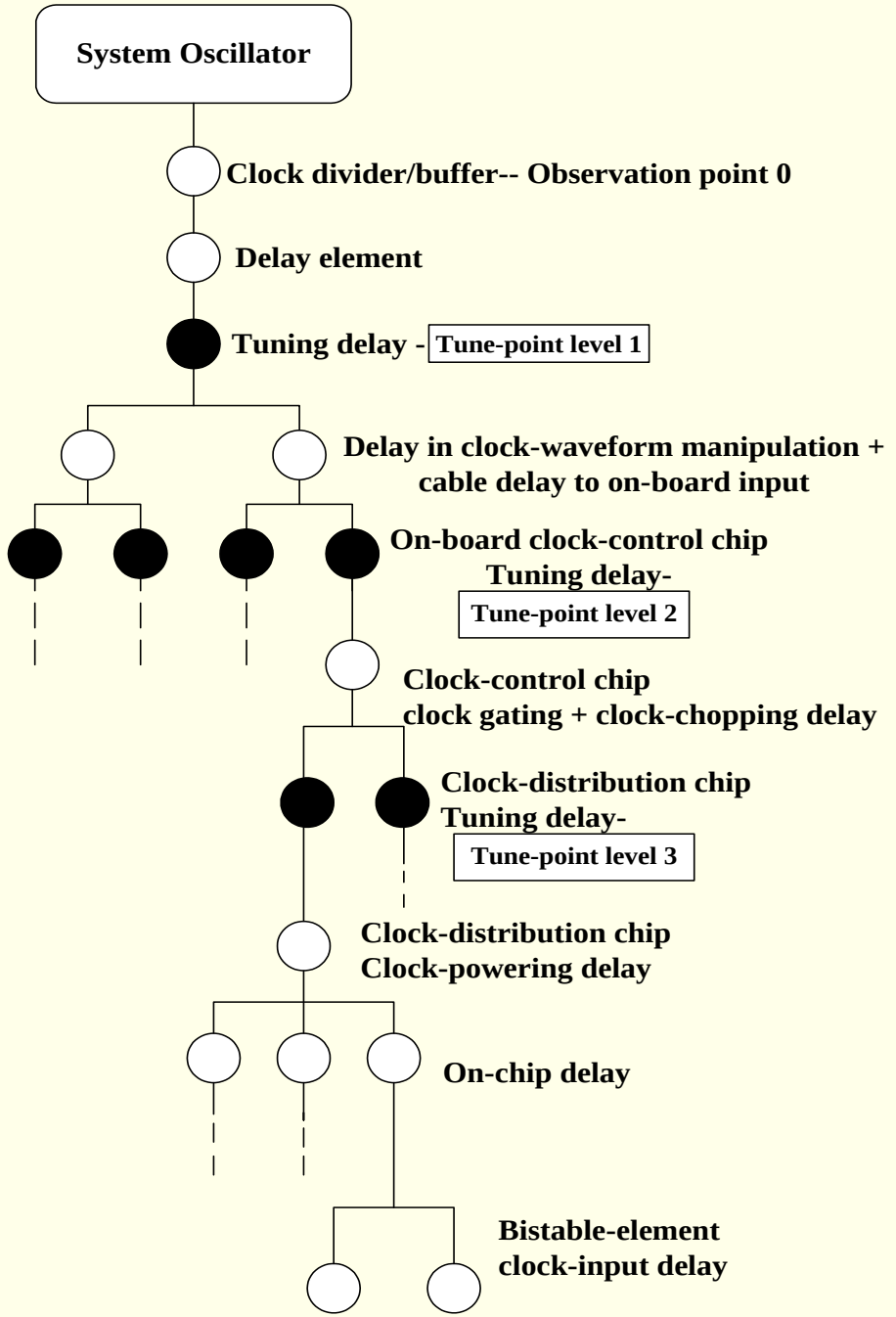

Various Clock Shaping Elements and Obtained Clock Signals.

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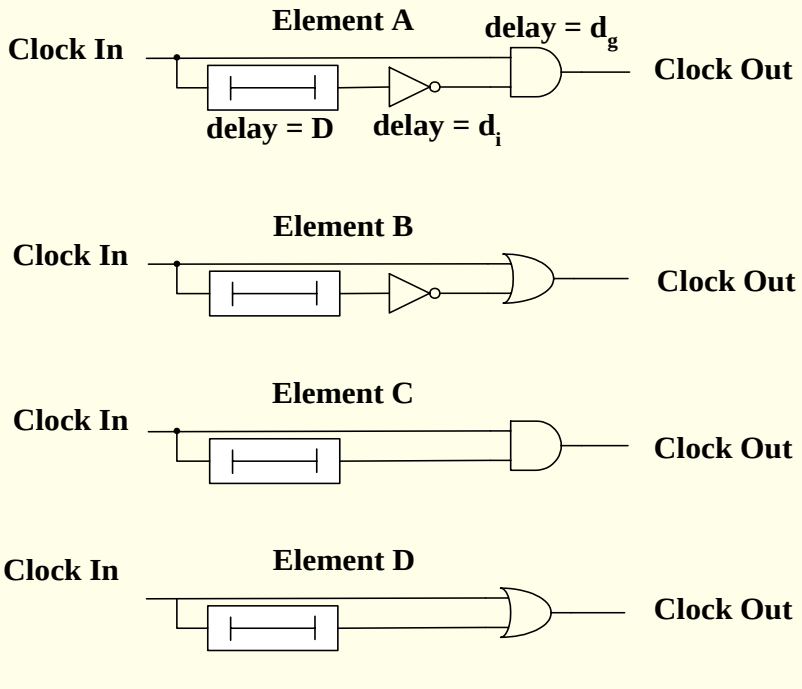
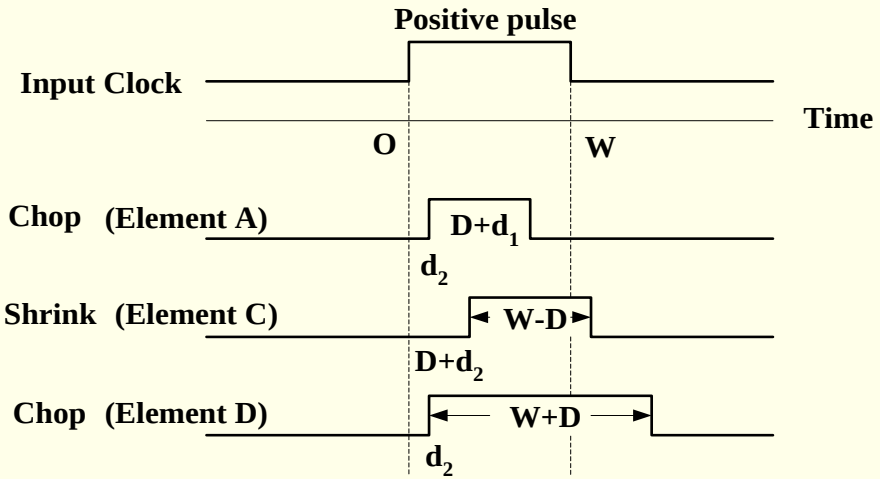
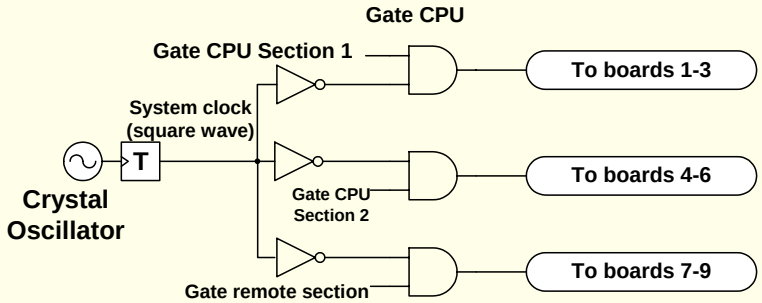


(a)



(b)

Clock distribution network
within a system,
(b) on the board, and
(c) tuning of the clock.
(Wagner 1988), Copyright © 1988 IEEE



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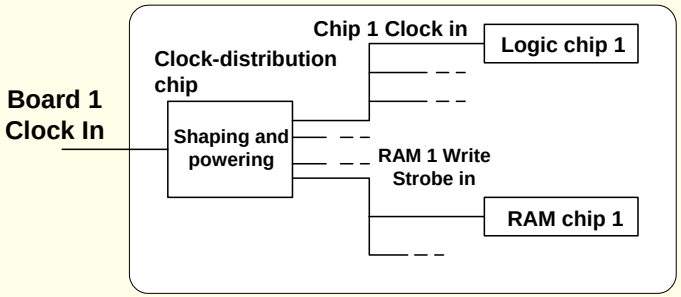
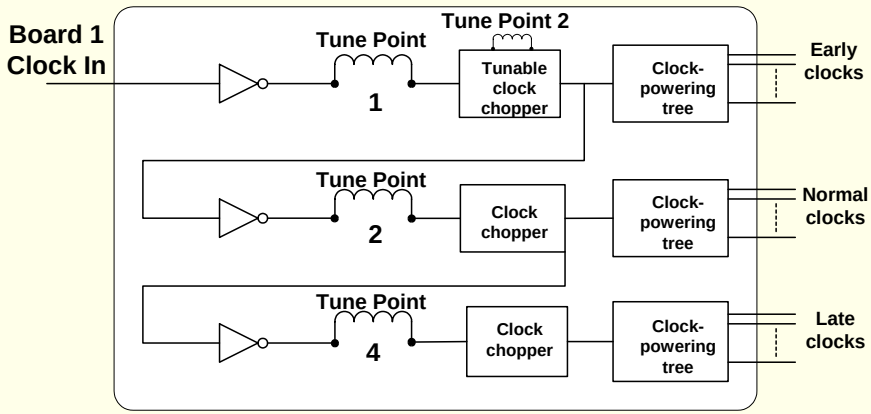


(b)

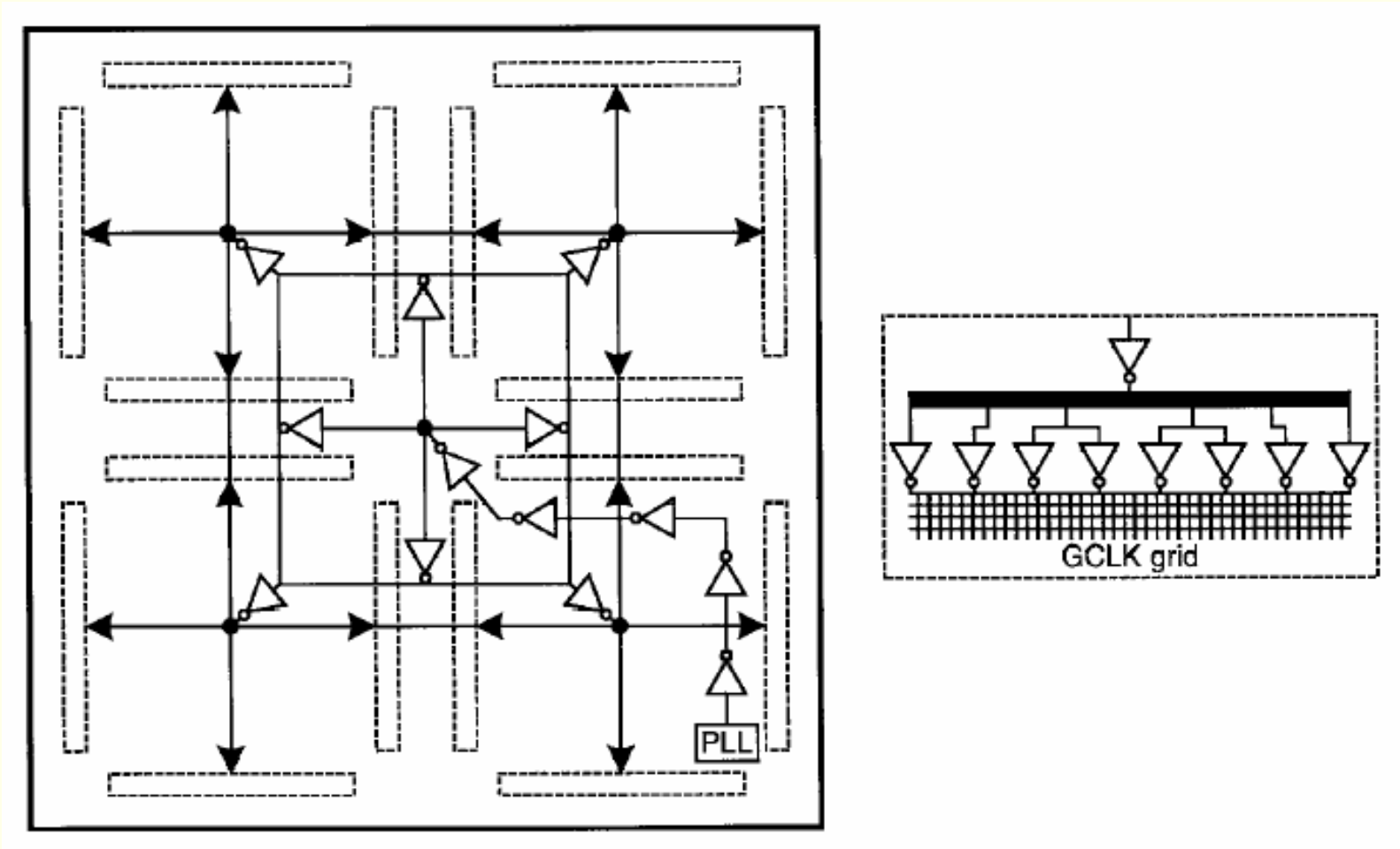


(c)

Clock distribution methods:

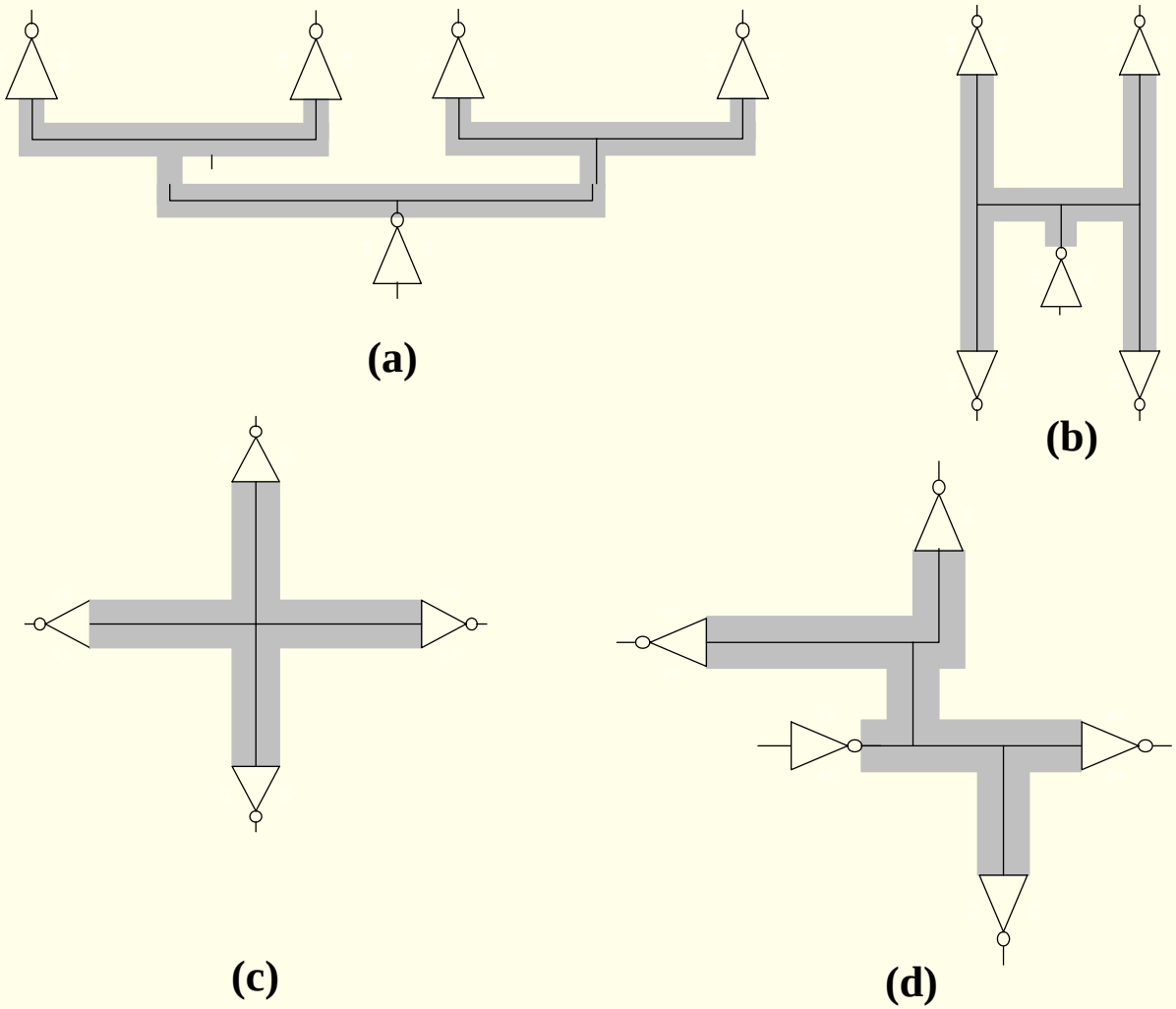
(a) an RC matched tree, and (b) a grid

(Bailey and Benschneider 1998), Copyright © 1988, IEEE



RC delay matched clock distribution topologies: (a) a binary tree, (b) an H tree, (c) an X tree, (d) an arbitrary matched RC matched tree

(From Bailey in Chandrakasan et al. 2001), Copyright © 1988, IEEE



Clock distribution grid used in a DEC Alpha 600-MHz processor

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